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DEVELOPMENT OF A MULTIKILOWATT ION THRUSTER POWER PROCESSOR

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16. Abstract

This program covers the feasibility study of applying the Silicon-Controlled Rectifier Series Resonant Inverter power conditioning technology to electric propulsion power processing operating from a 200 to 400Vdc solar array bus. A power system block diagram was generated to meet the electrical requirements of the JPL 20CM Hollow Cathode Mercury Bombardment Ion Engine. The SCR Series Resonant Inverter was developed as a primary means of power switching and conversion, and the Analog-Signal-to-Discrete-Time-Interval-Converter (ASDTIC) control system was applied to achieve good regulation. A complete breadboard was designed, fabricated and tested with a resistive load bank, and critical power processor areas relating to efficiency, weight and part count were identified.

The beam, accelerator and arc supplies which accounted for about 90% of the total power were integrated with a 20CM Ion Engine. Unusually reliable operation of the power processor with the ion engine was demonstrated resulting from the inherent capability of the Series Resonant Inverter to control the instantaneous current flow in the power components during overload modes and arcing of the Ion Engine. During the tests, a new ion engine fault clearing system was identified. When an overload is detected, the plasma density is reduced by reducing the arc reference current and thereby the load across the beam supply is cleared without a complete shutdown of the power processor.

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FOREWORD

This work is based on the series inverter and control system (ASDTIC) development work performed by Dr. F. C. Schwarz while at NASA Electronic Research Center. The work was started under Dr. F. C. Schwarz and Mr. Frank Raposa, formerly of the NASA Electronics Research Center, 575 Technology Square, Cambridge, Massachusetts, and completed under Dr. F. C. Schwarz and Mr. Howard Shumaker, NASA Lewis Research Center, Cleveland, Ohio.

We would like to thank Dr. Schwarz for his support and technical guidance in performing the power processor development, JPL Electric Propulsion Group for the loan of the 20CM Hollow Cathode Ion Engine, and Mr. E. V. Pollock of JPL for technical support in running the ion engine.

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1.0 SUMMARY

Prior to the work reported herein, the former NASA Electronic Research Center (NASA/ERC) successfully demonstrated the performance of a fixed input voltage, 95% efficient, 2kW series resonant inverter when operated as a beam supply for a 20CM ion engine. The objective of this work performed during the period of 1 July 1969 to 1 February 1970, and from 1 July 1970 to 1 November 1970 was to develop a basic power processing system for the various loads of a 20CM ion thruster using the series resonant inverter approach initiated at the NASA/ERC. The main effort was expended in the following areas:

- Power Processor Design
- Power Processor Breadboard Fabrication and Test
- Power Processor Breadboard Integration Testing
- Power Component Evaluation
- Analysis of Power Processor Baseline Electrical Stresses, Losses, Weight and Part Count
- Beam, Accelerator and Arc Supply Integration Testing with the Hollow Cathode Engine

Development work was done which improved the SCR power circuits, SCR control logic, output regulators and the command and protection system. Section 4, Block Diagram, documents all the detail block diagrams for the basic system, output regulator and the command and protection system. The Analog Signal to Discrete Time Interval Converter (ASDTIC) control system was incorporated into the design in order to meet the $\pm$0.1% regulation requirements for the magnet current, the arc current and beam output voltage. Section 5 documents the detail schematic diagrams of each subcircuit of the ion engine power processor.

The subcircuits were integrated and the complete power processing system breadboard performed satisfactorily with an overall breadboard efficiency of 88.6 to 89.4 percent at full load, and 86.2 to 86.6 percent at half load on the arc and beam supply, over the input voltage range of 200 to 400Vdc.

Testing of the SCR's was performed and critical component parameters which contribute to efficiency loss were evaluated.

The electrical stresses of the processor breadboard components were studied, and circuit and component modifications were made to maximize efficiency.

The baseline power processor breadboard losses, weight, and part count were analyzed and detail breakdowns are shown in Section 8 of this report.

The breadboard development was oriented to demonstrate the obtainable efficiencies and to verify by testing the compatibility of the beam, accelerator and arc supply characteristics with an engine.

The preliminary engine testing with the beam, accelerator and arc supplies has shown the excellent capability of the series resonant inverter electric power processor on initial turn on of the engine. The protection schemes required to protect against failure of the power conditioner in case of engine arcing, the clearing of shorts between the V5 and V6 electrodes, and the ability to return to normal operation without turning off any of the power supplies were demonstrated. The command and protection system can be simplified when using this type of power processor. Sequencing and time delaying of the various outputs during engine turn on or restart are not required for the protection of the series resonant inverter electric power processor and the command and protection system can be optimized strictly for the benefit of the engine.

2.0 INTRODUCTION

High power silicon-controlled rectifiers (SCR's) or thyristors have been used in high voltage and high power equipment for industrial applications for many years. The design objectives were primarily low cost and low maintenance as the design requirements of low weight and high efficiency for space equipment are usually not a factor in ground applications.

In space applications, the primary design requirements are high reliability and low weight. Power processor inefficiency results in spacecraft weight penalties due to increased power source capacity required to supply the additional power processor losses.

Future high power spacecrafts will be using high voltage distribution to minimize the cable weight and losses and will have high power loads such as electric propulsion, direct broadcast communications or other high power type loads or experiments.

Dr. F. C. Schwarz identified the basic advantages of the SCR series resonant inverter operating at high input voltage and high switching frequencies to reduce equipment weight without major penalty in efficiency and to provide reliable operation where the current is not subjected to transients when fault or overload conditions exist in an ion engine.

Dr. Schwarz, at NASA Electronics Research Center, designed a 2 kilowatt beam supply using the SCR series resonant inverter to operate off a 300V fixed input source. This unit was integrated with the 20CM ion engine and successful performance was demonstrated.

The objective of this program was to design, construct and test a multikilowatt ion engine power processor using the series resonant inverter as the basic power stage operating at 200 to 400Vdc input. The basic tasks to accomplish this objective were as follows:

1. Develop a detailed power processor block diagram showing the flow of power from the input to the output loads, the input command signals, control logic, overload protection signals and the telemetry signals. Interface requirements between all these functions were to be determined.

2. Design the required power and electronic control circuits utilizing the series resonant inverter as the primary means of power conversion. Utilize the Analog-Signal-to-Discrete-Time-Interval-Converter (ASDTIC) in the critical voltage and current regulation functions of the power processor. Series Resonant Inverter Silicon-Controlled Rectifier (SCR) sequencing and protection control logic is under development by NASA for operation over a variable input voltage range to be completed and adapted for use in the design of the ion engine power processor.

   NASA/ERC successfully demonstrated the performance of a fixed input voltage, 95% efficient, 2KW series resonant inverter when operated as a beam supply in conjunction with an ion engine. These tests clearly established its inherent ruggedness for all conditions of engine operation, including severe engine arcing or shorts.

3. Build and test the power and electronic subcircuits over specified input, output and temperature ranges. The construction of individual power supplies (with telemetry circuits) shall be such as to allow electrical integration of the individual subsystems.

4. Integrate the subcircuits into a complete ion engine power processor and test with a dummy load to show compatibility of the circuits.

5. Set up a hollow cathode engine and perform preliminary integration tests with the beam supply.

6. Perform analyses to gain a detailed knowledge of the distribution and magnitude of electric stresses in the power circuit components for purposes of component improvement and reliability redundancy analysis.

7. Translate the knowledge acquired under Item (6) into defining a program for the improvement of power circuit components and of the power system characteristics, including its power density and efficiency.

3.0 REQUIREMENTS

The requirements established as a goal for this development were as follows:

3.1 Electrical Requirements

3.1.1 Input

The power conditioner shall be compatible with a spacecraft solar cell array power source and provide stable operation of the 20cm JPL mercury ion thruster. For design purposes a 300V input was considered the nominal voltage, and the normal input voltage variation for which the power conditioner should satisfy the output requirements specified was 200 to 400V. The power conditioner should remain operating below 200V (with out-of-tolerance outputs permissible) but would automatically shut off at or below 180V.

The solar cell array is an inherent unidirectional power source and is current limited. The power conditioner should not supply reverse current to the input power source. Any network of filtering necessary to assure compatibility with the solar cell array power source was to be a part of the power conditioner.

3.1.2 Outputs

The power conditioner electrical output requirements are a function of the ion thruster input requirements and its operating characteristics. Fig. 3-1 shows a block diagram of the power conditioning system. The following subparagraphs present the detailed power conditioner output requirements. Electrical outputs are defined in Table 3-I and Table 3-II.

3.1.2.1 Electromagnet and Manifold Heater Supply No. 1

The supply shall be capable of providing the requirements listed in Table 3-I and Table 3-II.

The No. 1 supply provides power to the electromagnet and manifold which are connected in series. The resistance of the electromagnet is expected to be as follows:

(a) Cold Resistance: $R_{25°C} = 4.5\Omega$

(b) Hot Resistance: $R_{200°C} = 8.0\Omega$

22 AWG Copper wire is being used.

The inductance of the electromagnet is 7 mH.

The power requirement of the manifold heater is 7 watts at 0.67 amperes. The manifold heater utilizes 80Ni-20Cr wire with a negligible temperature coefficient. The resistance value of the heater is 14Ω and remains practically constant throughout the operating temperature range. The supply shall be designed to provide a maximum of 16 watts or 19 volts at 0.85 amperes for continuous operation.

3.1.2.2 Main Vaporizer Supply No. 2

Output requirements for supply No. 2 are given in Table 3-I and Table 3-II. The load resistance is 5Ω (dc) and remains practically constant throughout the full range of operating temperature. Supply No. 2 will be current limited and will operate at the spacecraft ground potential.

The power supply shall be current limited and shall be self-protected against overloads.

Supply No. 2 shall operate closed loop with the beam power supply No. 5.

The feedback signal in this loop shall be derived by sensing I_5 current.

An externally supplied reference signal, I_{BRef} (see paragraph 3.1.5) will be compared to the feedback current I_5.

Figure 3-2 defines the closed loop performance.

If proportional control is used, then the positive error signal ΔI_5 will control the output of the No. 2 supply (Figure 3-1).

3.1.2.3 Cathode Vaporizer Supply No. 3

The supply shall be capable of providing the requirements specified in Table 3-I and Table 3-II.

The load resistance is $16.5 \pm 0.5\Omega$ (dc) and remains practically constant throughout the full range of operating temperature. PS-3 will be current limited; it will operate at 2kV above-ground potential, and shall be self-protected against overloads.

Supply No. 3 shall operate in closed loop with the arc power supply No. 4 (paragraph 3.1.2.4).

This loop is the major loop. Another, minor, current loop is provided that maintains the output current constant and equal to the preset reference value I_{3Ref}. The I_{3Ref} covers the range of 0.8A to 1.0A (Figure 3-3).

Initially, after the thruster is ignited, the major servo loop is opened (i.e., $E_4 > E_{4Ref}$) and the supply No. 3 operates at the constant current mode (Figure 3-3).

The major servo loop closes when E_4 drops below E_{4Ref} because the arc current I_4 has reached the level of reference I_{4Ref} (Figure 3-4) and PS-4 has started to operate in the current limited region.

This loop is self-compensating which means that lowering of E_4 causes a reduction of I_3 and a reduction of Hg vapor within the arc, resulting in a rise of E_4.

The E_{4Ref} shall be adjustable from 32V to 35V.

3.1.2.4 Arc Supply No. 4

Supply No. 4 shall be capable of providing the requirements specified in Table 3-I and Table 3-II.

The supply shall be capable of supplying a load floating at 2000V above ground.

The specified value of E_4 shall be provided at the thruster terminals. The anticipated line resistance amounts to 1.5Ω.

In view of the fact that the arc power supply carries the sum of the arc and beam currents, the "true" arc current shall be derived from the sensor placed in the negative arc return line, as per Figure 3-1.

The arc supply requires two modes of operation: (a) startup, and (b) normal closed loop operation. These are discussed separately. The E-I characteristic is shown in Figure 3-4.

(a) Startup: For startup, in order to initiate a discharge within the thruster ionization chamber, a minimum of 150Vdc open circuit with a short circuit capability of at least 20mA shall be provided.

(b) Normal Operation: Once a discharge has been initiated an uninterrupted voltage transition to the lower level of operation is required.

The open loop E/I characteristic of the supply is shown in Figure 3-4a. The exact shape of the characteristic shall be at the discretion of the designer, providing that the output voltage at the thruster terminals at 10A in all cases is not lower than 36V.

A variable current limit will be provided; by means of I_{4Ref} the true arc current shall be limited within 2A to 10A. The current limited mode of operation is shown in Figures 4b and 4c. Whereas in Figure 3-4b current limit has been set for I_4 = 2A (i.e., $f(I_{4R})$ = 0V), in Figure 3-4c I_4 = 10A (i.e., $f(I_{4R})$ = 5V).

The operating point will settle at a voltage level defined by E_{4R}. For example, in Figure 4b, E_{4R} = 33V, and, in Figure 4c, E_{4R} = 34V. The range of E_{4R} setting shall be 32-35V, as further described in Figure 3. The slope of the current limit shall be approximately $\Delta E_4/\Delta I_4$ = 400[V/A].

Arc supply No. 4 shall operate in closed loop with the cathode vaporizer supply No. 3. This major loop shall force PS-4 to operate in the current limited mode at the voltage level determined by the E_{4Ref}. This reference shall be presettable to 32 to 35V. For further details see paragraph 3.1.2.3.

3.1.2.5 Beam Power Supply No. 5

The supply shall be capable of providing the requirements specified in Table 3-I and Table 3-II.

A minor servo loop shall keep the output voltage constant within 1.0% for line voltage and load current variations specified.

Supply No. 5 will operate closed loop with the vaporizer supply No. 2 as described in paragraph 1.2.2. (Also see Figure 3-5.)

The current sensor of I_{5F} Bk (see Figure 3-1) shall be compensated, so as not to measure the accelerator current that circulates through PS-5.

3.1.2.6 Accelerator Supply No. 6

The supply shall be capable of providing the requirements specified in Tables 3-I and 3-II.

A minor servo loop shall keep the sum of the output voltages $E_4+E_5+E_6$ constant within 0.1% for line voltage of 200 to 400V over load current variations as follows: I_4 = 2 - 10A, I_5 = 0.5 - 1.0A, I_6 = 5 - 10mA.

3.1.2.7 Neutralizer Cathode-Vaporizer Supply No. 7

The supply shall be capable of providing the requirements listed in Table 3-I and Table 3-II. It should be noted that upper and lower current limiting shall be provided: the lower limit shall be 0.3A or less, the upper current limit shall be internally adjustable within 3.0 to 3.8A range. Supply shall be capable of supplying a load floating at 100V below the ground.

The output of the No. 7 supply shall be controlled by a voltage feedback signal from the output of the No. 8 supply. This signal will be compared to a voltage reference (E_{8Ref}) and the error signal generated will be used to control the output current. E_{8Ref} shall be internally adjustable to allow presetting E_8 anywhere within the range 10V to 20V.

In addition, another feedback loop which permits operating supply No. 7 at constant current will be provided. The I_7 current feedback will be compared to a current reference (I_{7Ref}) and the error signal will keep I_7 at a constant, preselected value. The range I_{7Ref} will be internally adjustable to preset I_7 within 3.0A and 3.8A. The two loops will be designed so that the voltage loop will have priority over the current loop.

The control characteristics shall be such that the constant output current I_7 will be maintained until E_8 drops below E_{8Ref}; below this value of E_8, the current I_7 will be reduced proportionally to 0.3A (RMS): this will be accomplished by means of an error signal ($E_{8Ref} - E_8$) (see Figure 3-6).

Slope $\Delta I_7/\Delta E_8$ (Figure 3-6) shall be approximately 1A/V.

3.1.2.8 Neutralizer Keeper Supply No. 8

The supply shall be capable of providing the requirements specified in Table 3-I and Table 3-II. An output isolation of 200V shall be provided for bias operation. The neutralizer keeper supply requires two modes of operation:

(a) Initiating a discharge, and (b) Normal operation.

(a) Initiating a discharge - For startup and initiating a discharge in the neutralizer a minimum of 200Vdc at 5mA with a short circuit capability of 20mA shall be provided. Once a discharge has been initiated an uninterrupted voltage transition to the normal operating level shall be provided.

(b) Normal operation - The normal operation of the neutralizer keeper supply requires 50V at 20mA with a source impedance such that the output drops to zero volts dc with a neutralizer keeper current of 550mA $\pm$ 5%. (See Figure 3-7.)

The operating point lies in the vicinity of 550mA in the constant current region.

This supply operates in a closed loop with supply No. 7, as described in paragraph 3.1.2.7.

3.1.2.9 Cathode Tip Heater Supply No. 9

The supply shall be capable of providing the requirements specified in Table 3-I and Table 3-II.

The load resistance is 4 $\pm$ 0.1Ω (dc) at 1000°C. Tungsten wire is used for this heating element.

The power supply shall be current limited and be selfprotected against overloads. It does not need to be of a regulated type; tap changing can be used in order to increase the output power to 12V/3A if required.

A signal from the power supply No. 4 shall be capable of turning the PS-9 OFF. The level at which this occurs shall be presettable within I_4 = 3 to 9A (see Figure 3-8).

PS-9 shall be turned back ON, whenever the arc current drops below minimum value. This value shall be presettable with I_4 = 1 to 3A. The turn-on shall occur only if the condition persists for more than five seconds. This provision shall blank out the response of the loop to the discontinuities of arc current during the temporary shut-downs after arcing.

3.1.2.10 Cathode Keeper Supply No. 10

The supply shall be capable of providing the requirements specified in Table 3-I and Table 3-II.

Supply requires two modes of operation: (a) initiating a discharge and (b) normal operation; requirements for (a) are identical with these defined for PS-8; requirements for (b) differ. In the low voltage region supply will operate at the constant current, as preset by the I_{10Ref}.

3.1.2.11 Bias Power Supply No. 11

This supply is not part of the power conditioning equipment but part of the laboratory power system. Supply furnishes a dc voltage within a 10 to 100V range and carries the emission current, I_E (Figure 3-1).

3.1.2.12 Preheating of the Power Conditioner

Heater elements shall be mounted within the power conditioner for the purpose of maintaining the temperature of the components above -50°F during the period when the power conditioner is turned off but exposed to -300°F cold plate in vacuum.

Heaters shall be capable of dissipating 200W of heat from 115V, 60Hz, 1 ph source.

One temperature sensor shall be installed within the power conditioner to regulate the temperature to -50°F.

A second temperature sensor shall be installed with the power conditioner to remove the ON-2 INHIBIT (see paragraph 3.1.4.3) when the temperature of 0°F is exceeded.

A third temperature sensor shall be provided for indicating the actual temperature of the power conditioner.

Preheating shall be initiated manually, after the pump down of the vacuum chamber and cooling of the cold wall is started. Temperature of the power conditioner shall be maintained at -50°F by means of an externally installed ON/OFF regulator. Temperature of the power conditioner shall be raised automatically, by ON-1 CMD, until it exceeds the 0°F level, where the ON-2 INTERLOCK shall be removed.

After an ON-2 CMD is given, preheating of the power conditioner shall be discontinued.

3.1.3 Overload Response

It is necessary that each individual supply shall be protected against excessive current.

It shall be the design objective that all the supplies shall be short circuit proof and shall not be overloaded even by a permanent short. Each supply should be capable of operating with any such load without causing any component to exceed the temperature allowed by reliability assessment of the component.

In addition, supplies 5 and 6 shall be equipped with an undervoltage detector that initiates a temporary shutdown in case of a sustained arc between grids. The shutdown shall occur only if the undervoltage condition persists for a period longer than approximately 100ms. Undervoltage is defined as a voltage below 90% of the nominal value.

3.1.4 Startup and Shutdown

3.1.4.1 Commands

The power conditioner will be activated from an external source by means of commands for operating relays. Each command shall have:

(a) Amplitude of 20 to 31Vdc
(b) Duration of 20ms or more
(c) Current capability of 100mA

All command lines will be at tank ground potential.

3.1.4.2 Interlocks

The interlock will consist of an open switch voltage of 5V nominal (35V maximum, 4V minimum). Closing the switch will remove the interlock. Drain will be 10mA at V_{CES} = 0.5V nominal (2.0V maximum).

3.1.4.3 Startup Procedure

(a) Set I_{BRef} to zero volts.

(b) Apply "ON-1 CMD", this will increase the heating power and raise the power conditioner temperature to 0°F, disabling the "ON-2 INHIBIT" interlock.

(c) Apply "ON-2 CMD." This will energize the Group I supplies. Wait for five minutes.

(d) Apply "ON-3 CMD." This will energize Group II supplies. The power conditioner is now ready to respond to I_{BRef} CMD.

(e) Set I_{BRef} at the desired value.

Note: The above individual commands will be given after verification of telemetry data delivered.

3.1.4.4 Shutdown Procedure

Two types of shutdowns may occur:

(a) Regular shutdown

(b) Emergency shutdown

Regular Shutdown

External relay commands will be generated by the controller to terminate normal operation. This procedure is aimed at eliminating any possible contamination of surfaces by condensation of mercury.

(a) "OFF 1 RELAY CMD" - Vaporizer supply No. 2 is turned off. Rate of delivery of mercury decays. Wait until beam current decays below one-half of the preset reference value.

(b) "OFF 2 RELAY CMD" - Turn off all supplies.

Emergency Shutdown

"OFF 2 RELAY CMD" - will be given, "OFF 1 CMD" will not be used.

3.1.5 Recovery from Arcing

Some of the arcs that occur within the thruster or between the thruster and the facility ground will not extinguish and must artifically be interrupted.

Shutdown of the thruster shall be initiated by one of the undervoltage detectors (see paragraph 1.3) of the supplies Nos. 5 or 6.

Such a signal shall shut down supplies Nos. 1, 2, 4, 5, 6.

After a delay, that can be readjusted within 50 and 500ms, power supplies Nos. 4, 5, and 6 shall be turned on.

The magnet power supply No. 1 shall be turned on after one second.

The main vaporizer power supply No. 2 shall be turned on after a preset delay of one to two seconds.

Should the arcing and restart occur after "OFF 1" was applied, restarting sequence will not nullify such command.

3.1.6 Analog Control of the Spacecraft

3.1.6.1 The analog signal required to command the spacecraft will be supplied in the form of I_{BRef} from a source with a maximum impedance of 1kΩ; maximum current drain from this source shall be less than 50μA. The value of this reference signal shall be continuously varied from 0Vdc (I_5 = 0.5A) to +5Vdc (I_5 = 1.0A). Figure 3-7 shows the steady-state transfer characteristics of the system. The command line shall be at power conditioner ground.

3.1.6.2 I_{4Ref} shall be derived from I_{BRef} by means of the function generator. The generated accuracy of the transfer curve (Figure 3-9)* shall be within ±0.5% of full scale. The curve shall reproduce 90% mass utilization.

Function generator shall be designed to perform during the mission time with a maximum predicted drift or deterioration of ±1/2% of full scale. High reliability of operation is essential. The possibility of a biasing scheme which could shift the curve up and down shall be investigated.

3.1.6.3 A switch at the output terminal of the function generator (see Figure 3-1) will be added in order to permit the introduction of an external I_4 reference.

*Will be supplied by JPL at a later date.

3.1.7 Telemetry Outputs

3.1.7.1 Amplitude

The power conditioner shall provide telemetry signals which shall continuously and linearly represent a given parameter from -0.5Vdc to 5.5Vdc, where zero volts and 5Vdc correspond to zero and 100% points, respectively.

Telemetry signals shall not, under any condition, exceed the range -2V to 7Vdc.

3.1.7.2 Source Impedance and Loading

The source impedance shall be 10kΩ or less.

The power conditioner shall not be inhibited from proper operation by telemetry loads (such as a short circuit) or by externally-induced telemetry-line noise or EMI.

3.1.7.3 Accuracy

Calibration accuracy of ±2% of full scale setting plus an additional ± 2% of the real value will be provided, with a maximum design drift of 1% over 10,000 hours of operation for all 0 to 5V telemetry signals, except as noted below.

Telemetry signals I_1, I_2, I_3, E_4, E_5, and E_6 must be of high accuracy. Over the temperature range 15°C to 75°C, these signals shall have a calibration accuracy equal to or better than one-half percent of actual value plus one-half percent of full scale for ranges specified in Table 3-II.

3.1.7.4 Grounding

The grounds for output power, chassis, commands, and telemetry shall be separated to allow for common connection at a remote point on the payload without the creation of ground loops. Power conditioner ground will be firmly connected to the tank ground.

3.1.8 Miscellaneous

3.1.8.1 Maximum voltage between the grids shall be less than 5kV for no-load to full load on the screen supply, and for 1mA to full load on the accelerator supply.

3.1.8.2 Rise time of voltages E_5 and E_6 should be as fast as feasible.

3.1.8.3 Toggle switches will be provided in order to modify the mechanization of the automatic recovery from an arcing (see paragraph 3.1.5) and to allow the substitution of automatic turn-on or turn-off of any of the power supplies Nos. 1, 2, and 4 with a manual one.

3.1.8.4 The rectifiers of the accelerator supply No. 6 will be capable of carrying the full screen current while the arcing between grids persists.

3.1.8.5 Because of an extremely high noise environment, great care in selection of various logic devices shall be applied. Wherever possible high threshold logic shall be used. Slow gates shall be given preference, but if not available, slow-down networks in all critical digital lines shall be added.

3.1.9 Design Criteria and Considerations

Consideration shall be given to the requirements of the over-all system at each step of the design and fabrication of the power conditioner. The Contractor should consider the following criteria, in the priority listed, in making the trade-offs required during design, manufacture, and test.

The criteria in sequence of importance are: efficiency, reliability, and weight.

TABLE 3-I

POWER REQUIREMENTS

Hollow Cathode - 20cm Thruster

Group	SUPPLY NO.	SUPPLY NAME	TYPE		MAXIMUM RATING			NOMINAL RATING					RANGE OF CONTROL	
					E	I	I_{LIM}	E	I	P	Regulation	Peak Ripple		
					V	A	A	V	A	W	%	%	A	
I	1	Magnet Manifold	DC		19	0.85	0.9	15	0.67	10.5	0.1 (I)	5	0.5-0.85 Preset by I_{1REF}	Constant Current
	7	Neutral Heater	DC		12	3.8	4	12	2.8	35	Loop	-	2-3.5	Set I_{REF} within 3.0-3.8A
	8	Neutral Keeper	DC		200 V 5 mA		0.55	20	0.5	10	1.0 (E)	2	-	Set E_{8REF} within 10-20 v
	9	Cathode Tip Heater	DC		12 v	3	4	8	2	16	5.0 (I)	-	0-3	
	10	Cathode Keeper	DC		200 V 5 mA	0.6	0.6	20	0.5	10	1.0 (E)	2	0.3-0.6 Set I_{10REF}	Constant current
II	2	Vaporizer Main	DC		10	2	2.2	7	1.4	10	Loop	-	0.5-1.5	Set I_{2REF} within 1.6-2.0A
	3	Cathode Vaporizer	DC		17	1.0	1.2	10	0.6	6	Loop	-	0.5-1.0	Set I_{3REF} within 0.8-1.0A
	4	Arc	DC		150 v 20 mA	10 36 v	12	34.5	9	310	0.1 (I)	2	2-10	I_{4R} sets current limit
	5	Beam	DC		2200 (1)	1.05	1.1	2 kv	1.0	20 kw	0.1 (E)	5	0.5-1.0	
	6	Accel.	DC		1100 (1)	0.1	0.2	1 kv	0.01	10	0.1 (E)	5	-	

(1) No load voltage, Max. permissible.

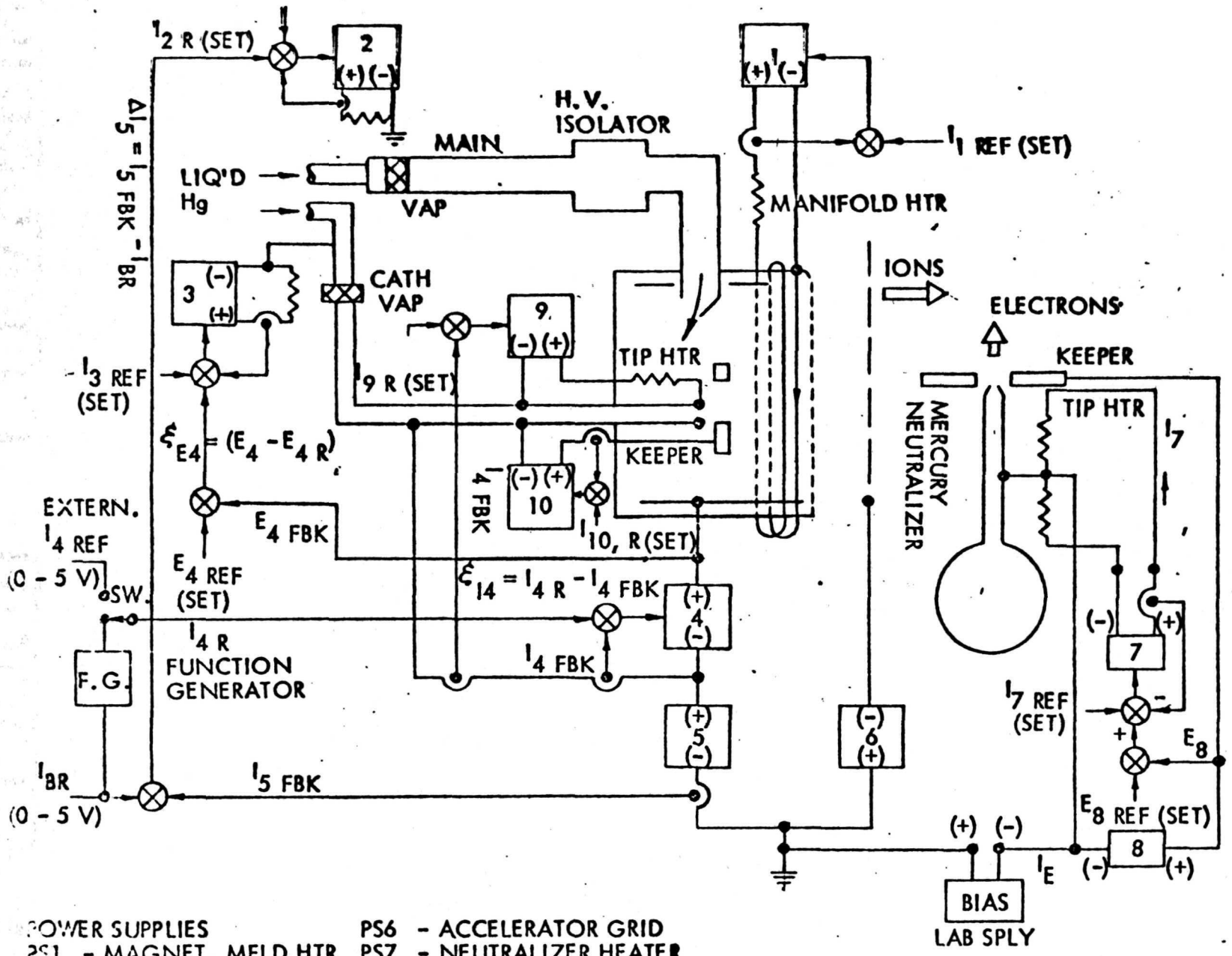
TABLE 3-II

TELEMETRY DATA

Supply #	Name	TELEMETRY			
		0 - 5 V Range		High Accuracy Part of TM Range	
		Current	Voltage	Current	Voltage
1	Magnet	0.3 - 0.9 A	----	0.50 - 0.75 A	----
2	Vapor. Main	0 - 2 A	----	----	----
3	Vapor. Cath.	0 - 1.2 A	----	----	----
4	Arc	0 - 10 A 1)	30 - 40 V 2)	2 - 9 A 1)	34 - 36 V 2)
5	Beam	0 - 1 A	1700 - 2100	0.5 - 1 A	1950 - 2050
6	Accel.	0 - 10 mA		----	
7	Neutr. Htr.	0 - 4 A	----	----	----
8	Neutr. Keeper	0 - 0.6 A	0 - 30	----	----
9	Cath. Tip Htr.	0 - 4 A	----	----	----
10	Cath. Keeper	0 - 0.6	----	----	----

NOTES: 1) MUST MEASURE TRUE ARC CURRENT.

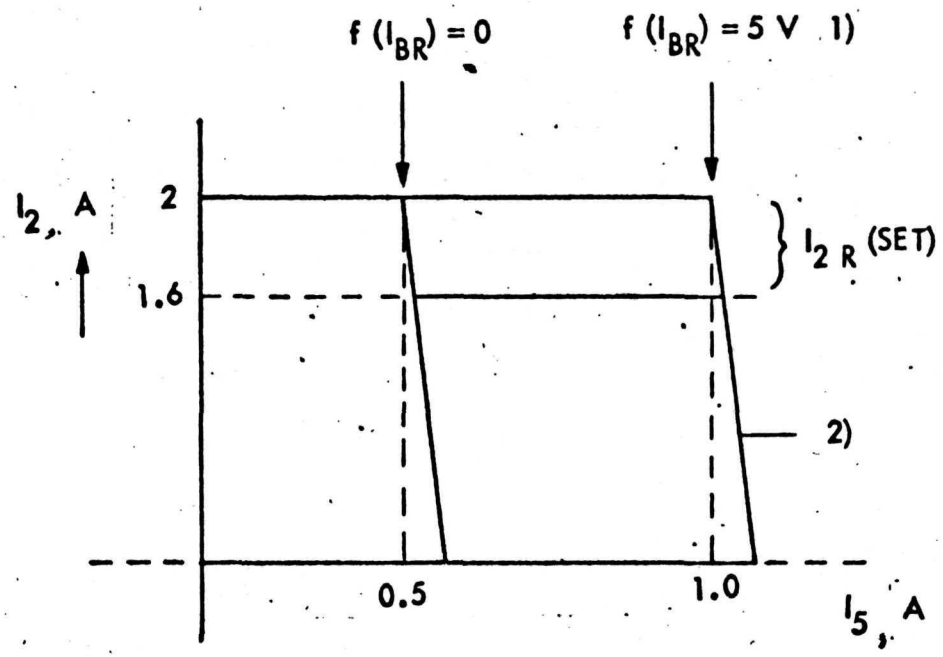
2) VOLTAGE AT THE THRUSTER END.



POWER SUPPLIES

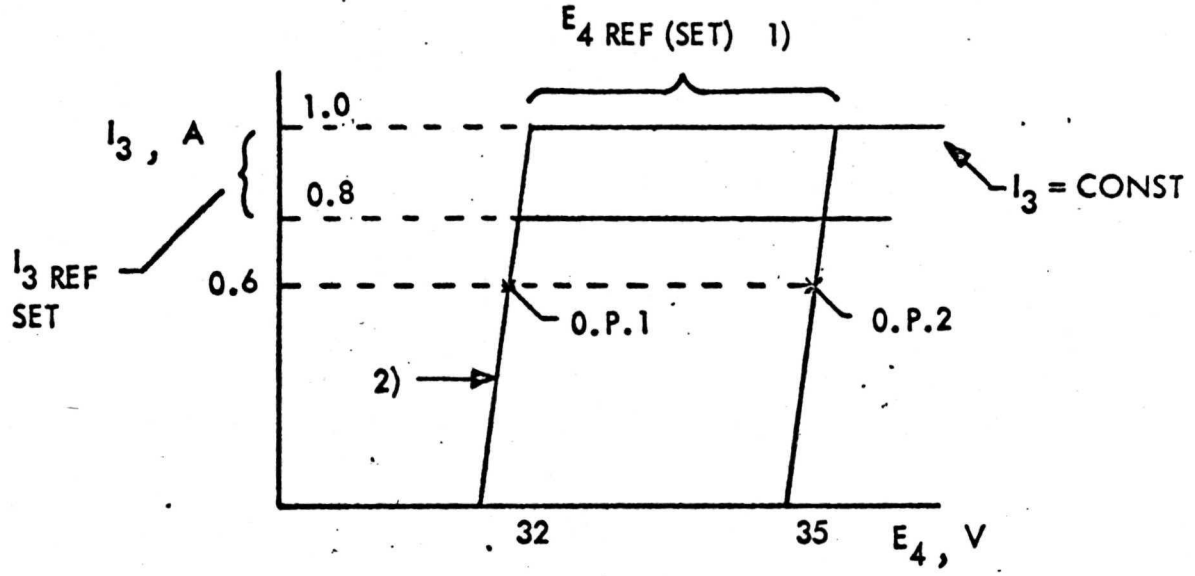
PS1 - MAGNET, MFLD HTR	PS6 - ACCELERATOR GRID
PS2 - VAPORIZER MAIN	PS7 - NEUTRALIZER HEATER
PS3 - VAPORIZER CATH	PS8 - NEUTRALIZER KEEPER
PS4 - ARC	PS9 - CATHODE TIP HEATER
PS5 - SCREEN (BEAM)	PS10 - CATHODE KEEPER
	PS11 - BIAS LAB SUPPLY

Fig. 3-1. 20CM THRUSTER HOLLOW CATHODE P.C. CONTROL LOOPS



1) POINT AT WHICH I_2 DROPS RAPIDLY IS CONTROLLED BY I_{BR} · AT $I_5 < I_{BR}$: I_2 = CONST
2) SLOPE $\Delta I_2/\Delta I_5 = 400 \left[{}^{A}/_{A}\right]$

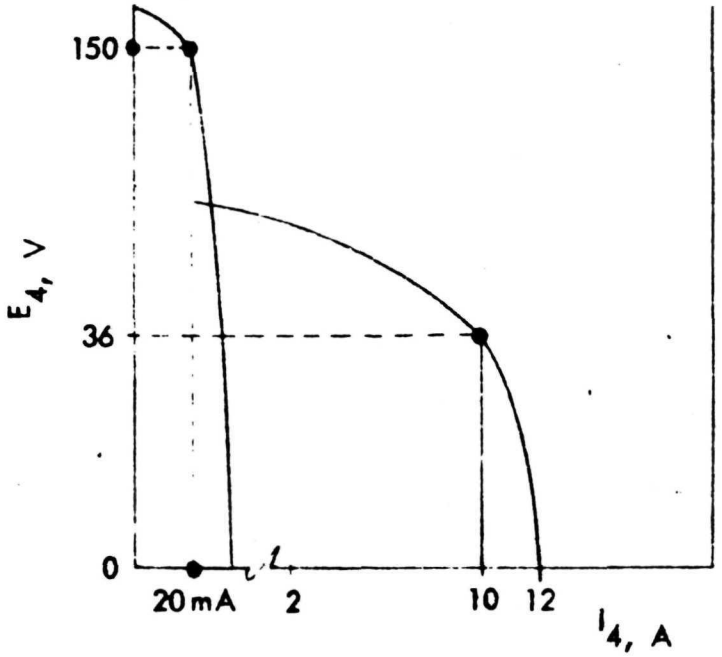
Fig. 3-2. CHARACTERISTICS OF SCREEN-VAPORIZER SERVO LOOP.



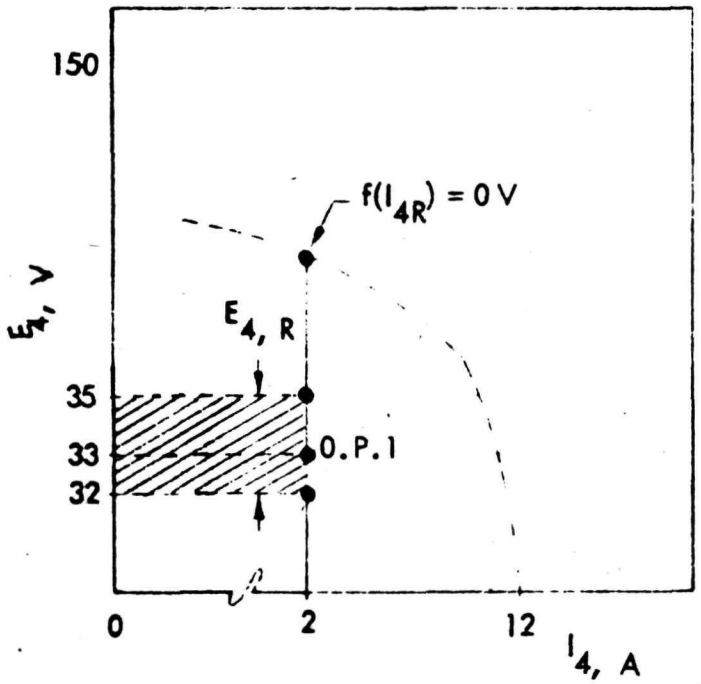
1) POINT AT WHICH I_3 RAPIDLY DROPS IS PRESET BY $E_{4\ REF}$, AT $E_4 > E_{4\ REF}$ I_3 = CONST
2) SLOPE $\Delta I_3/\Delta E_4 = 3 \left[A/V\right]$

Fig. 3-3 CHARACTERISTICS OF ARC CATHODE SERVO LOOP

(a) OPEN LOOP CHARACTERISTIC



(b)



(b) and (c)
CURRENT LIMITED MODE
OF OPERATION

(c)

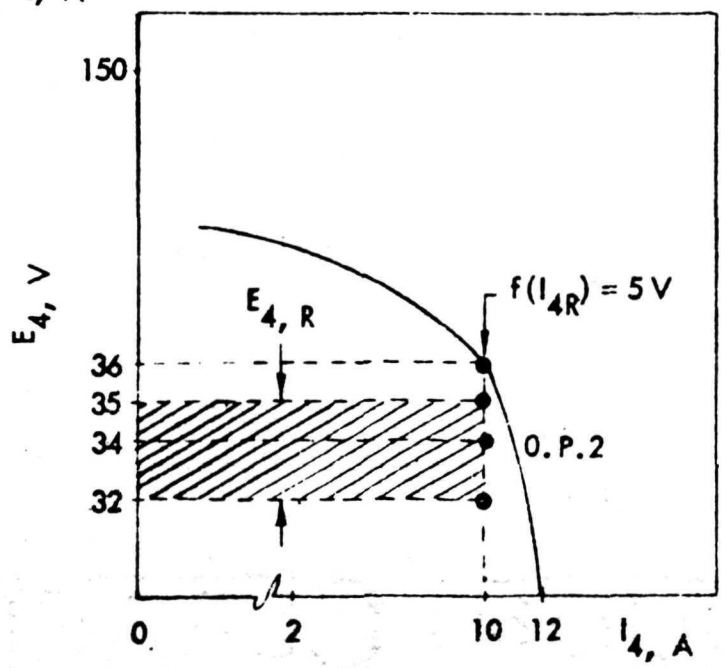


Fig. 3-4 E-I CHARACTERISTICS
OF THE ARC POWER SUPPLY No. 4

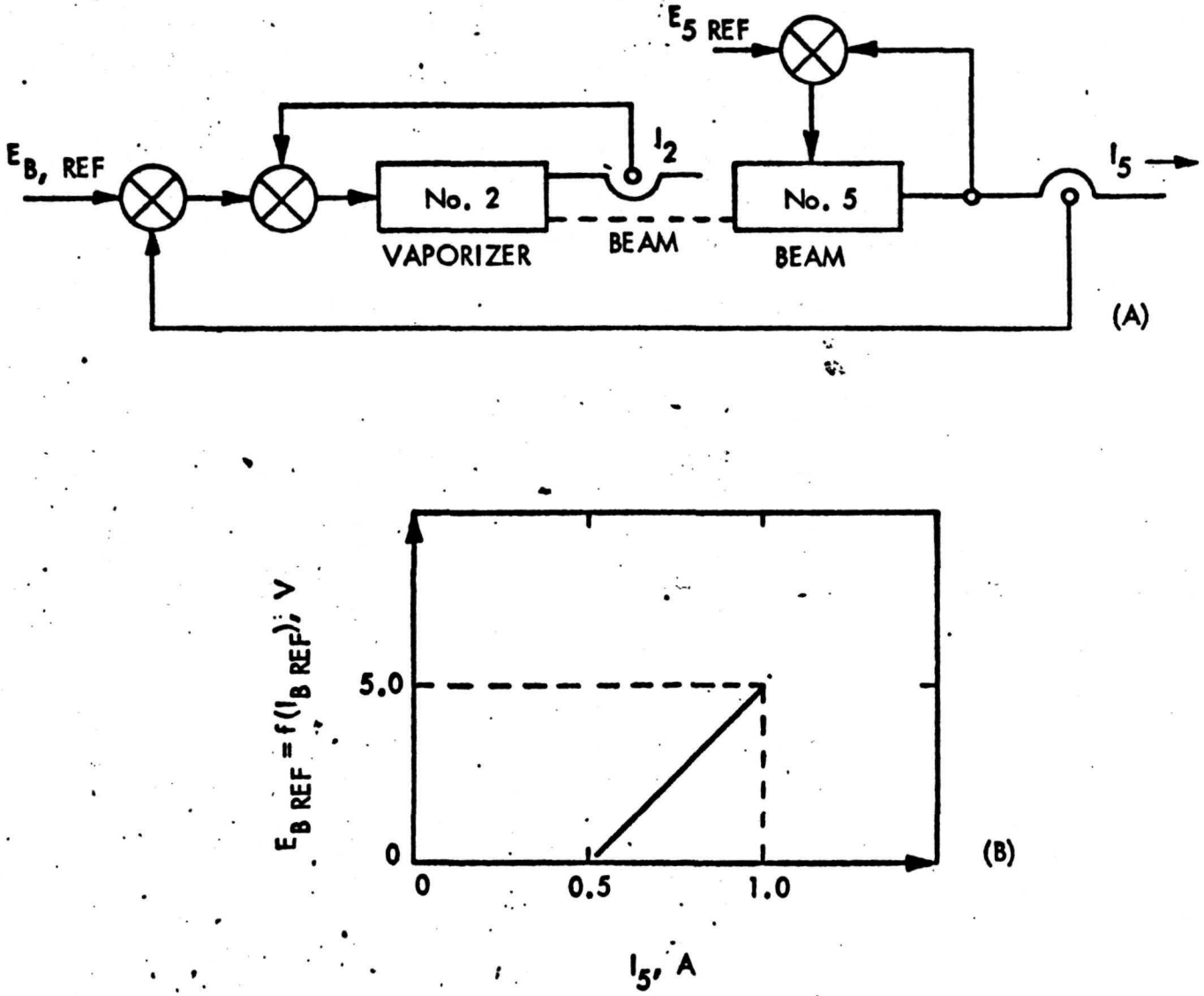


Fig. 3-5. VAPORIZER/BEAM SUPPLIES CLOSED LOOP RELATIONSHIPS

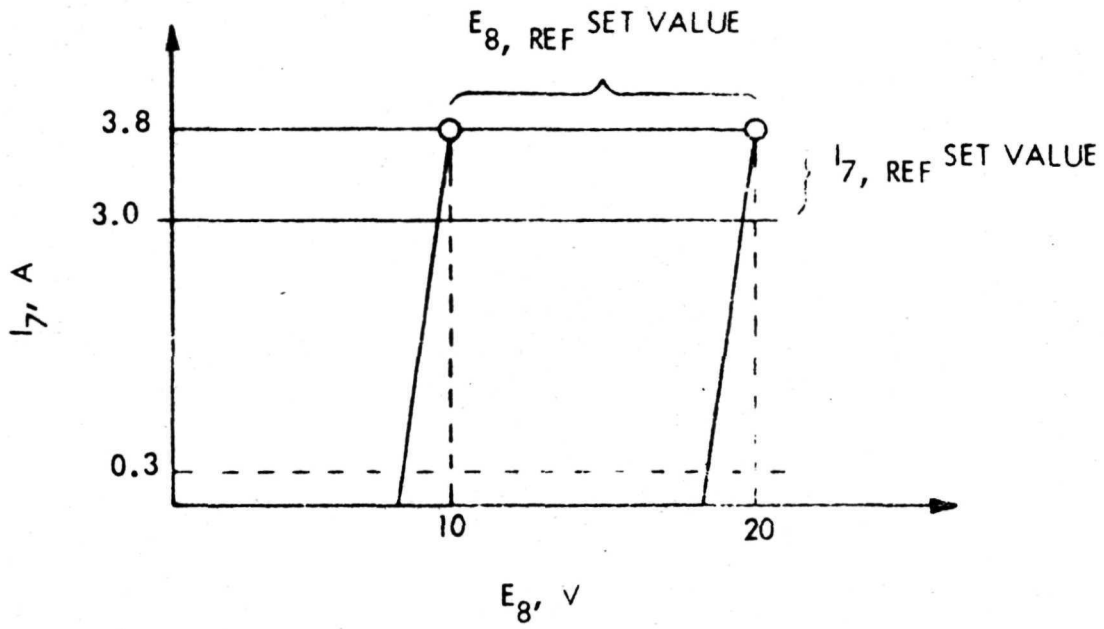


Fig. 3-6. SERVO LOOP CHARACTERISTICS OF NEUTRALIZER SYSTEM

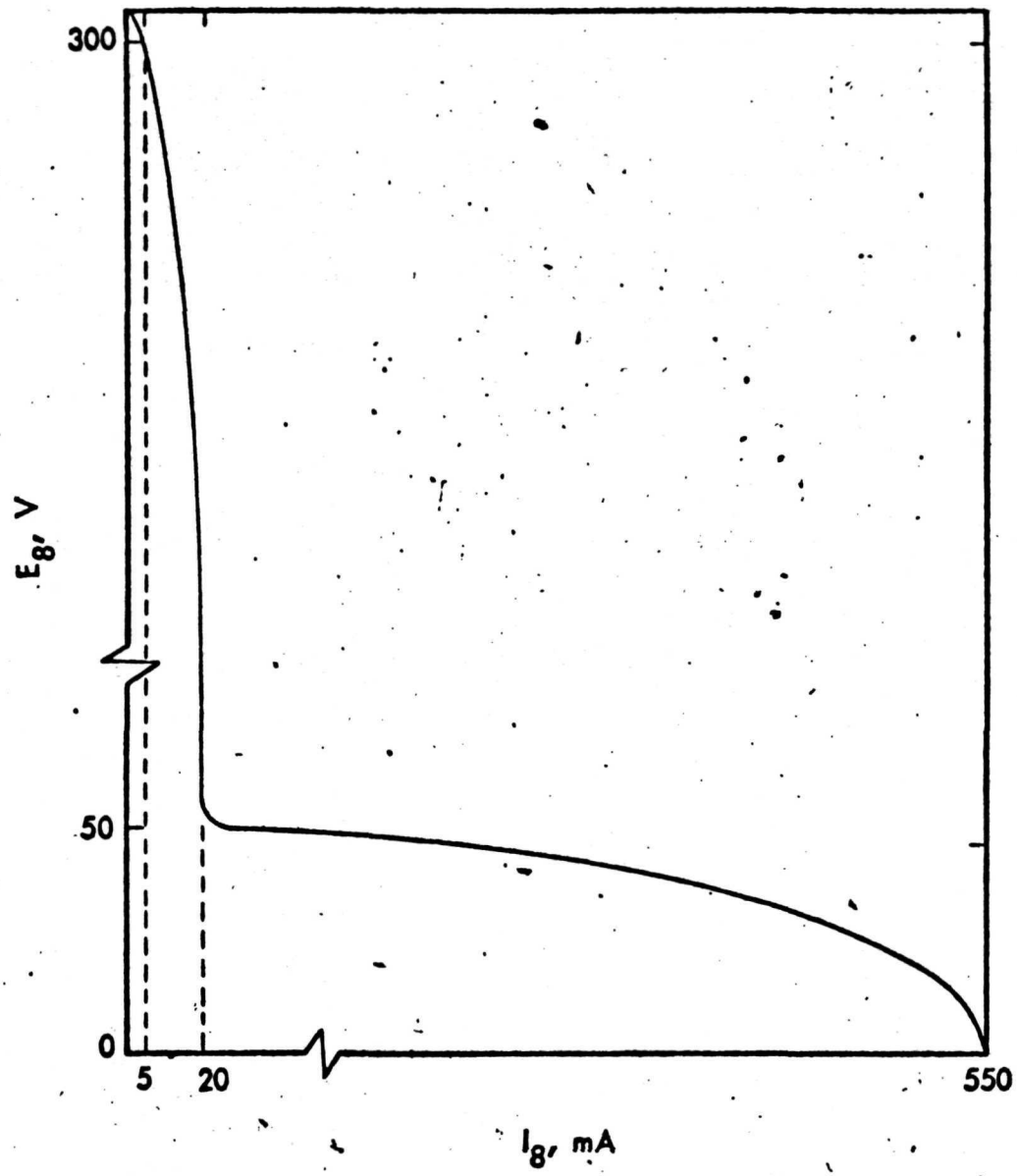


Fig. 3-7. NEUTRALIZER KEEPER SUPPLY, No. 8

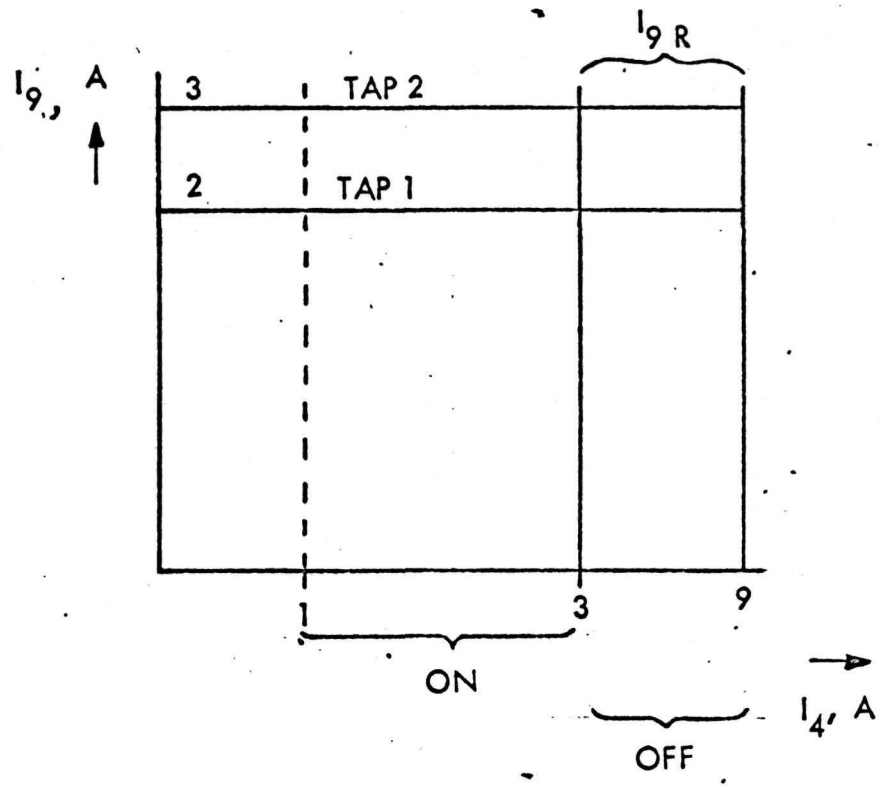


Fig. 3-8. ON/OFF CONTROL OF PS 9

4.0 BLOCK DIAGRAM

4.1 System Block Diagram

Figure 4-1 represents the block diagram mechanization of the electrical requirements of the ion thruster power processor. It can be divided into three basic areas.

- o The power circuit
- o The command and protection circuit
- o The output regulator circuitry

The mechanization of the system is influenced by the following items:

- o Engine control functions during startup, during normal operation and during overload,
- o Use of the SCR series resonant inverter power stage
- o Maximize efficiency
- o Maintaining all control electronics at ground potential
- o System grounding philosophy.

The heavy darkened lines show the flow of the 200V to 400Vdc solar array power through a common input filter into three SCR series inverters.

The input filter design consisted of a two-state LC network for filtering the high ac current drawn by the inverters to 1% RMS. The filter design was such that the filter Q was under 1.4 without causing any loss in filter efficiency. A common input filter was used to reduce the total filter weight of the power processor. It was expected that there will be some minor cross-coupling between the three inverters because of the common input filter, however, the regulator action of the three inverters were expected to eliminate this modulation from appearing in the output loads.

Series inverter No. 1 is the multiple output inverter. It feeds a fixed average current to all its loads which are connected in series. This inverter supplies the following loads:

- o PS 1 Magnet Supply
- o PS 2 Vaporizer Supply
- o PS 3 Cathode Heater Supply
- o PS 4 Arc Start Supply

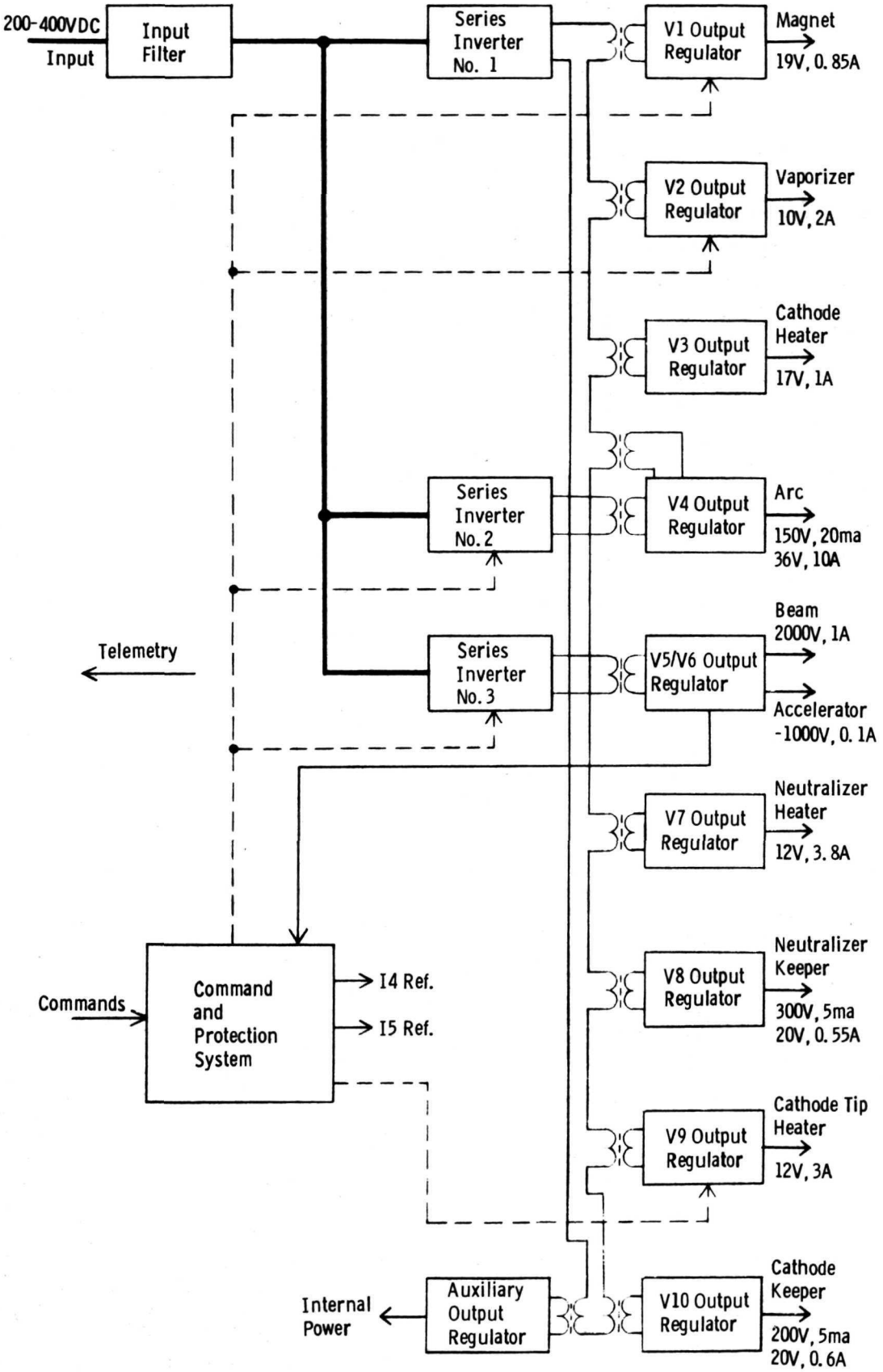


FIGURE 4-1. POWER PROCESSOR BLOCK DIAGRAM

- o PS 7 Neutralizer Heater Supply
- o PS 8 Neutralizer Keeper Supply
- o PS 9 Cathode Tip Heater Supply
- o PS10 Cathode Keeper Discharge Supply
- o Internal Auxiliary Supply

The total power rating of the inverter is about 200 watts.

Series inverter No. 2 powers only the PS 4 output (the Arc Supply) and has a power rating of about 400 watts.

Series inverter No. 3 supplies the PS 5 and PS 6 outputs (beam and accelerator) and has a power rating of about 2200 watts.

4.2 Output Regulators

All the active control loops are shown in simple block diagram form in Figure 4-1 to show the power and command interfaces. Detailed block diagrams are given in the following sections for all the regulating loops. Detail schematics are shown in Section 5.

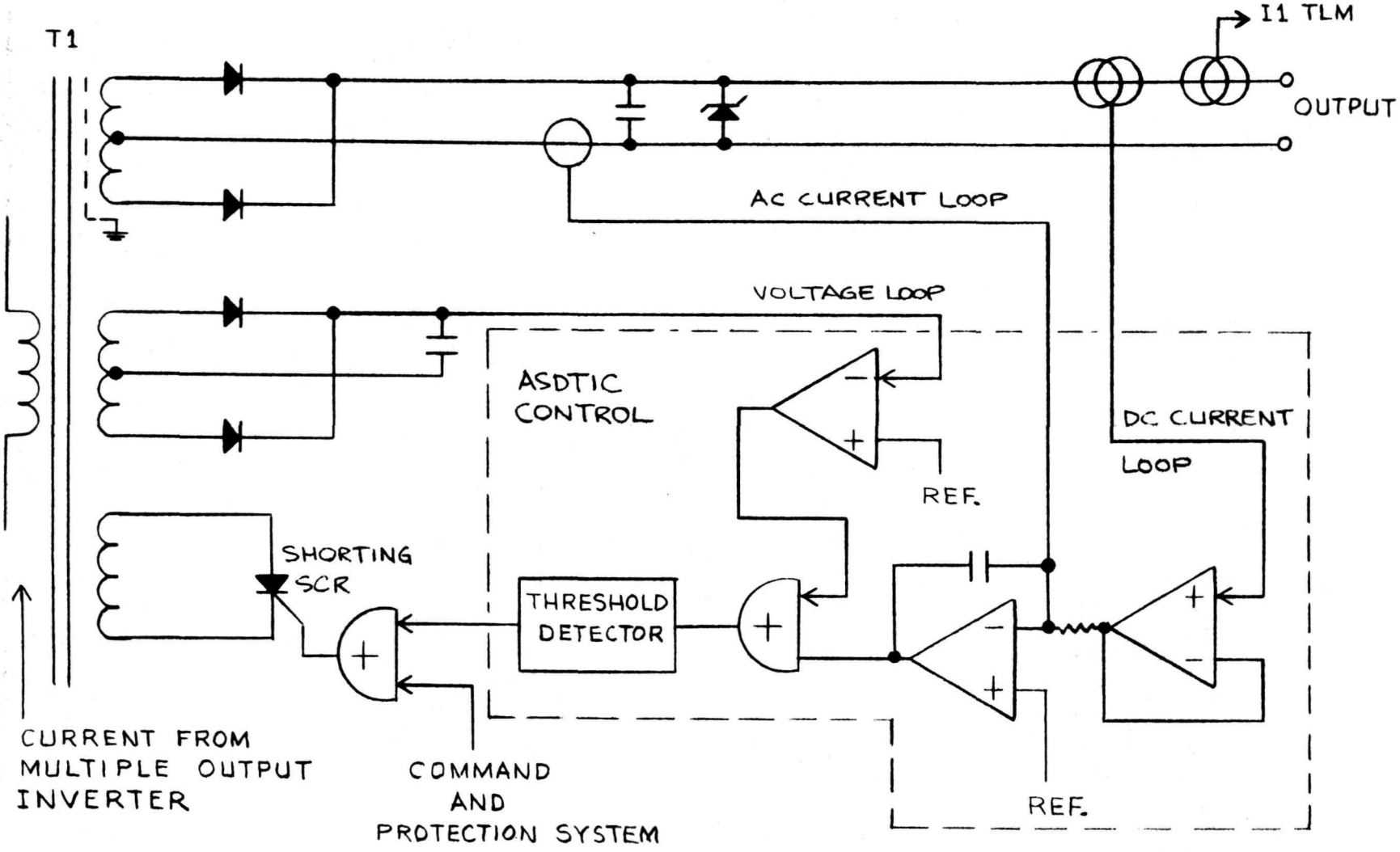


FIGURE 4-2 V1 - MAGNET POWER SUPPLY BLOCK DIAGRAM

4.2.1 PS-1, Magnet Supply

Figure 4-2 shows the block diagram. Current from the multiple output inverter excites the primary of transformer T_1. The main output of T_1 has 2000V insulation between primary and secondary. There are two regulating loops, a voltage control loop and a current control loop. The voltage loop controls the maximum value of the output and commands the shorting shunt SCR. The current regulating loop utilizes the ASDTIC (analog signal to discrete time interval converter) (ref. 1) principle to perform the system regulation.

The primary current is converted to a dc voltage signal via the primary current transformer and integrated by the operational amplifier. To correct for output regulation, a dc current transformer measures the actual output current and modifies the output of the integrating operational amplifier to meet $\pm$0.1% accuracy. This system allows high dc gain to be used in the amplifiers while maintaining stable regulator loop characteristics.

4.2.2 PS-2, Vaporizer Supply

Figure 4-3 details the control system for this supply. This supply has three regulating loops.

- V_2 voltage limiting
- I_2 current limiting
- I_5 current control

The first two loops are for maximum current and voltage limiting. The third loop controls the ion engine beam current flow by varying the power applied to the vaporizer. The beam current loop incorporates the ASDTIC amplifier for control.

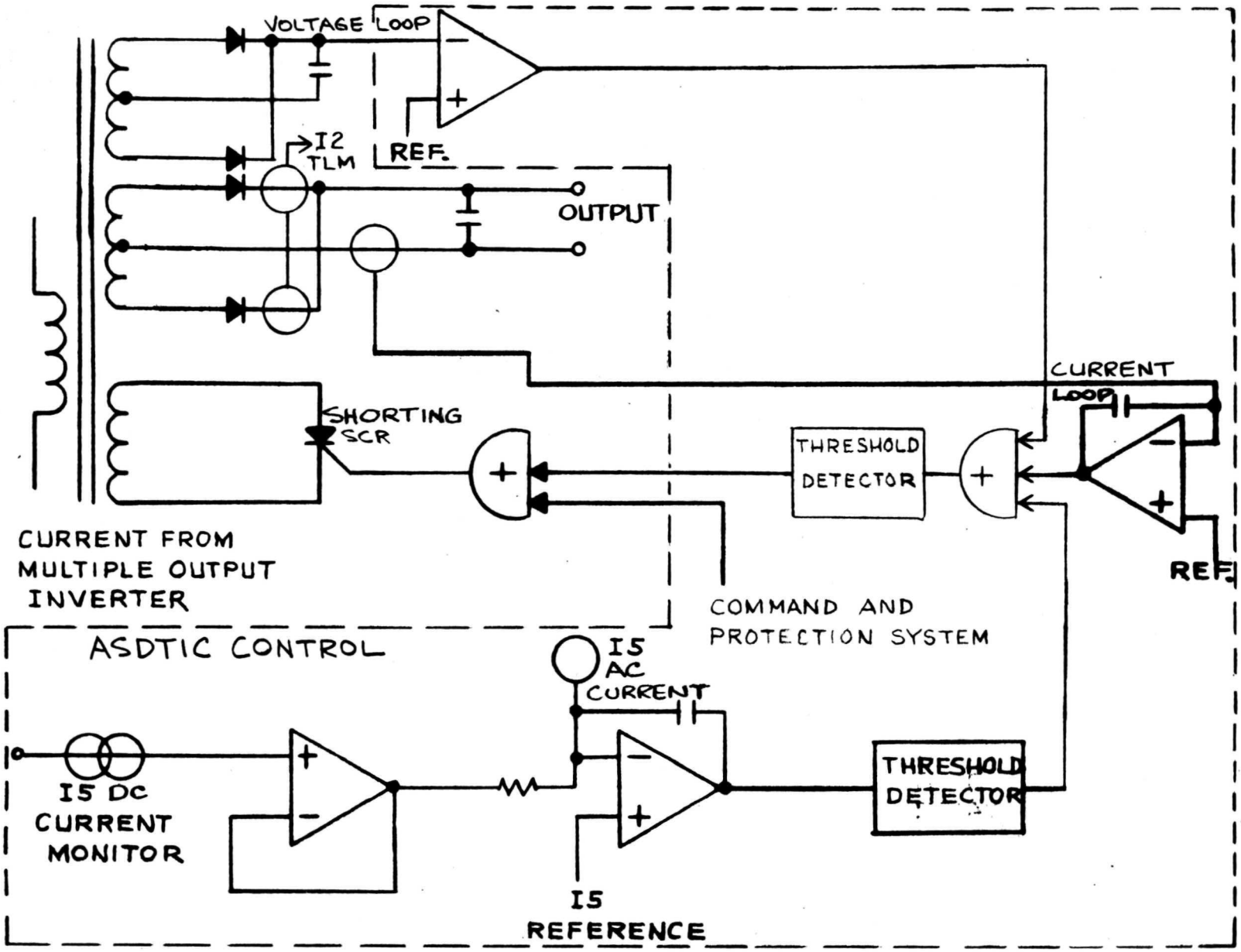


FIGURE 4-3 V2 - VAPORIZER POWER SUPPLY BLOCK DIAGRAM

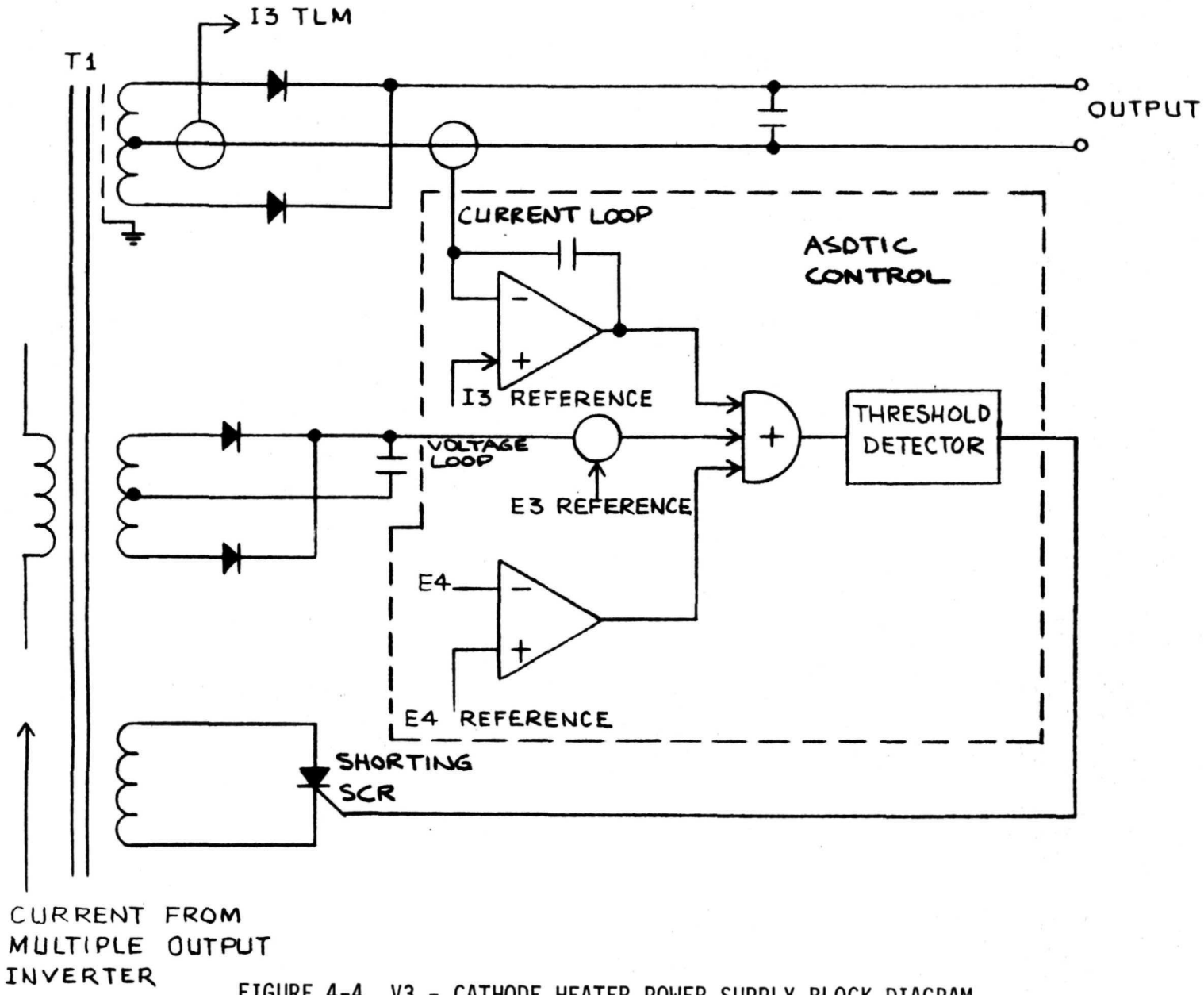


FIGURE 4-4 V3 - CATHODE HEATER POWER SUPPLY BLOCK DIAGRAM

4.2.3 PS-3, Cathode Heater Supply

Figure 4-4 is the block diagram. Transformer T_2 provides 2000 volt insulation. The supply has three control loops.

- V_3 voltage limiting
- I_3 current limiting
- V_4 voltage regulator

The first two loops control the maximum voltage and current output. The third loop actually controls the operation of the ion engine arc source.

4.2.4 PS-4, Arc Supply

Figure 4-5 is the block diagram for the arc supply. The main power is obtained from series inverter No. 2 through transformer T_1. Transformer T_2 supplies the high voltage (at low current) required to ignite the arc supply. This supply has two feedback loops.

- V_4 voltage limiting
- I_4 current regulation

The first loop limits the maximum output voltage across transformer T_1. The command reference current I_5 goes into the function generator and generates the I_4 reference for the current regulation loop of the arc supply. The current regulating loop incorporates the ASDTIC amplifiers for control. The output of the amplifier determines the frequency of operation for series inverter No. 2.

4.2.5 PS-5 and PS-6, Beam and Accelerator Supplies

Figure 4-6 is the block diagram for this supply. Series inverter No. 3 supplies the total output power for this supply. Two regulating loops are included.

- V_5, and V_6 output regulation
- I_6 overload control

The voltage regulation loop incorporates the ASDTIC amplifier which has a major and a minor feedback loop. In the major feedback loop, the total output voltage is sensed. In the minor loop, capacitor ac current is sensed. The output signal from the threshold detector is transformer coupled to the SCR inverter control logic to provide isolation between the input and output power ground.

The I_6 current limiting loop limits the amount of energy that can flow into the accelerator output (V_6).

4.2.6 PS-7, Neutralizer Heater Supply

Figure 4-7 is the block diagram for this output.

It includes three feedback loops.

- I_7 current limiting
- V_7 voltage limiting
- V_8 voltage regulation

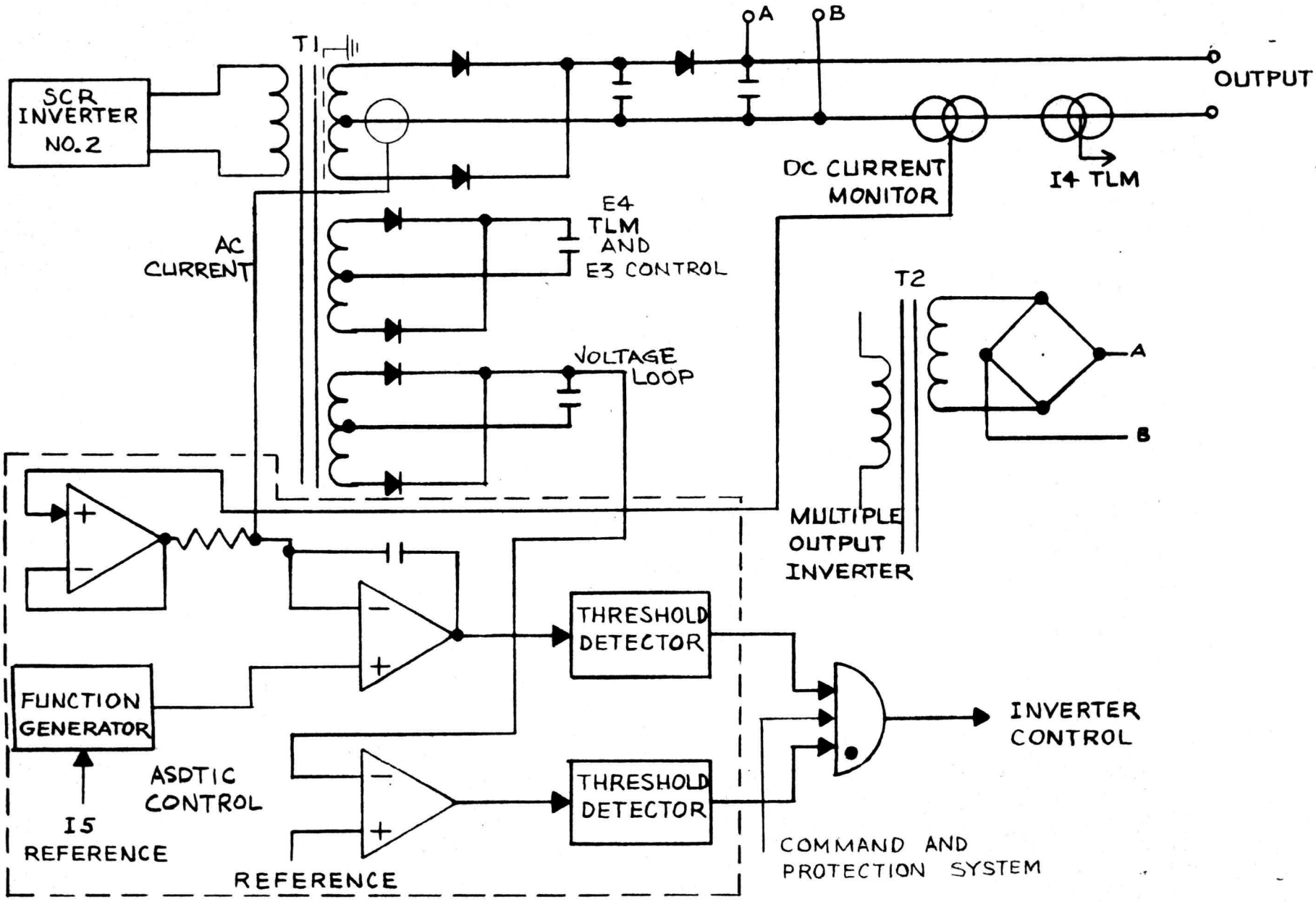


FIGURE 4-5 V4 - ARC POWER SUPPLY BLOCK DIAGRAM

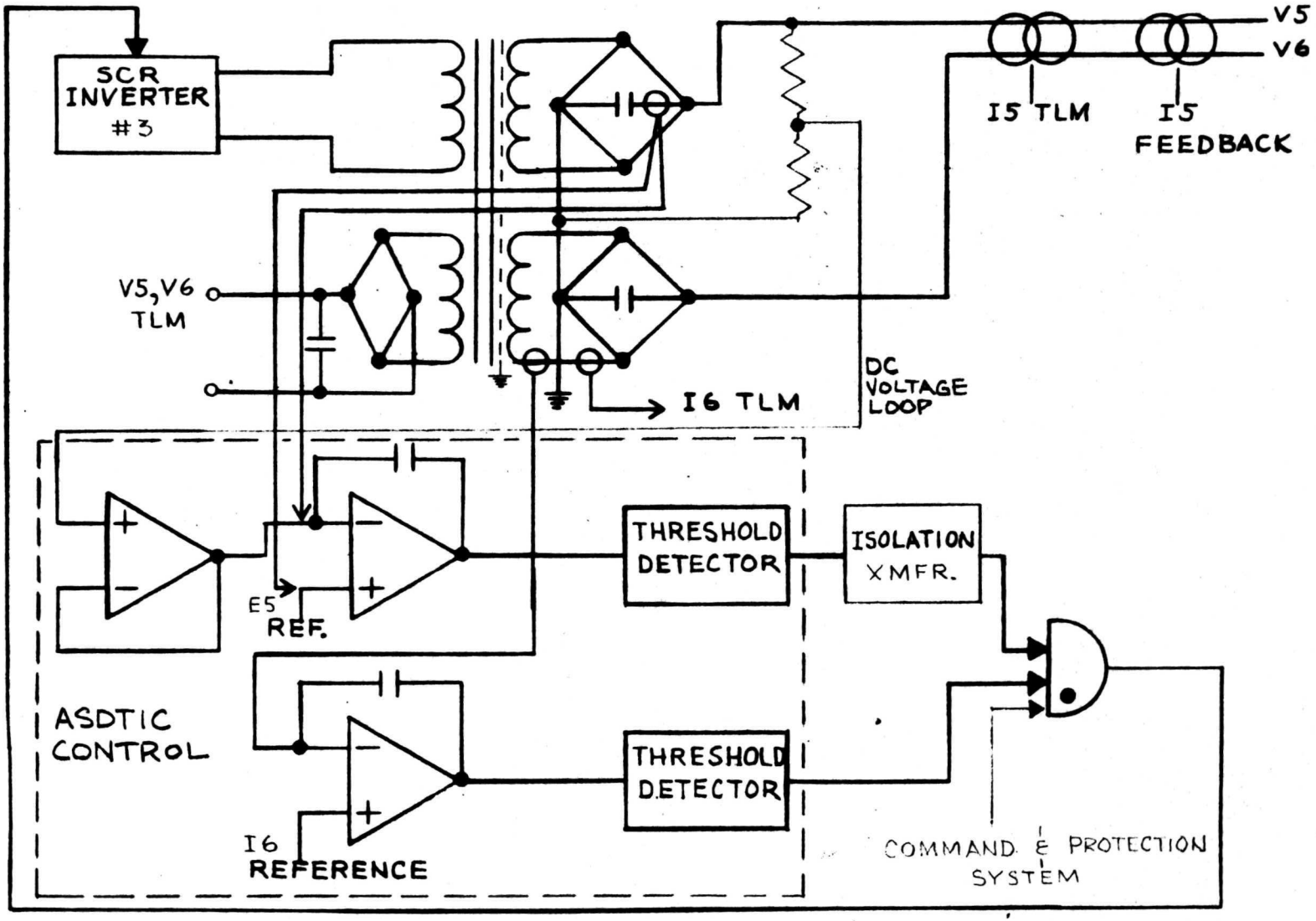


FIGURE 4-6 V5 AND V6 - BEAM AND ACCELERATOR POWER SUPPLY BLOCK DIAGRAM

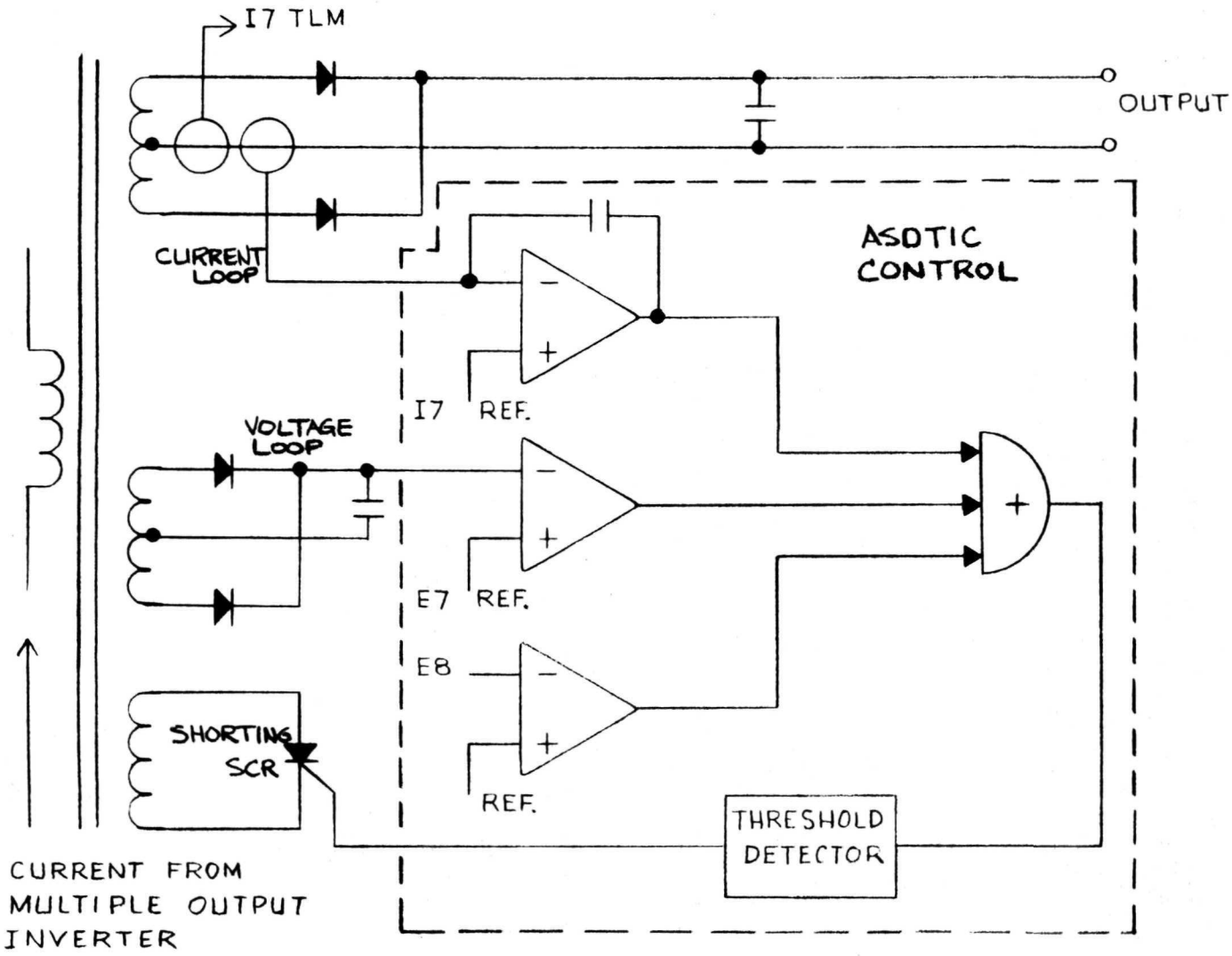


FIGURE 4-7 V7 - NEUTRALIZER HEATER POWER SUPPLY BLOCK DIAGRAM

The first two loops limit the maximum output voltage and current of the supply. The V_8 voltage regulation loop controls the performance of the neutralizer.

4.2.7 PS-8, Neutralizer Keeper Supply

Figure 4-8 is the block diagram for the neutralizer keeper supply. Transformer T_1 supplies the main output power while transformer T_2 supplies the high voltage (at low current) for the discharge supply. The regulator includes voltage and current limiting loops.

4.2.8 PS-9, Cathode Tip Heater Supply

Figure 4-9 is the block diagram for this supply. It includes a current and voltage limiting regulator. The current level of I_4 is sensed and if it is greater than a reference level it sets a flip-flop which turns the power supply off. If I_4 is below a different reference value and remains for a fixed time period, the flip-flop is reset and the system is allowed to return to normal operation.

4.2.9 PS-10, Cathode Keeper Supply

Figure 4-10 is the block diagram for this output. Transformer T_1 supplies the main output power. Transformer T_2 provides the high voltage (at low current) for generating a discharge.

4.2.10 Internal Auxiliary Supply

Figure 4-11 is the block diagram for this output. The output voltage of the transformer is held constant by the regulator. There are two isolated sets of 20 Volt outputs. One set is common to the input power ground and the second set is common to the output control circuit ground.

An additional set of diodes separate the power to the multiple output control logic to isolate the two power circuit during startups.

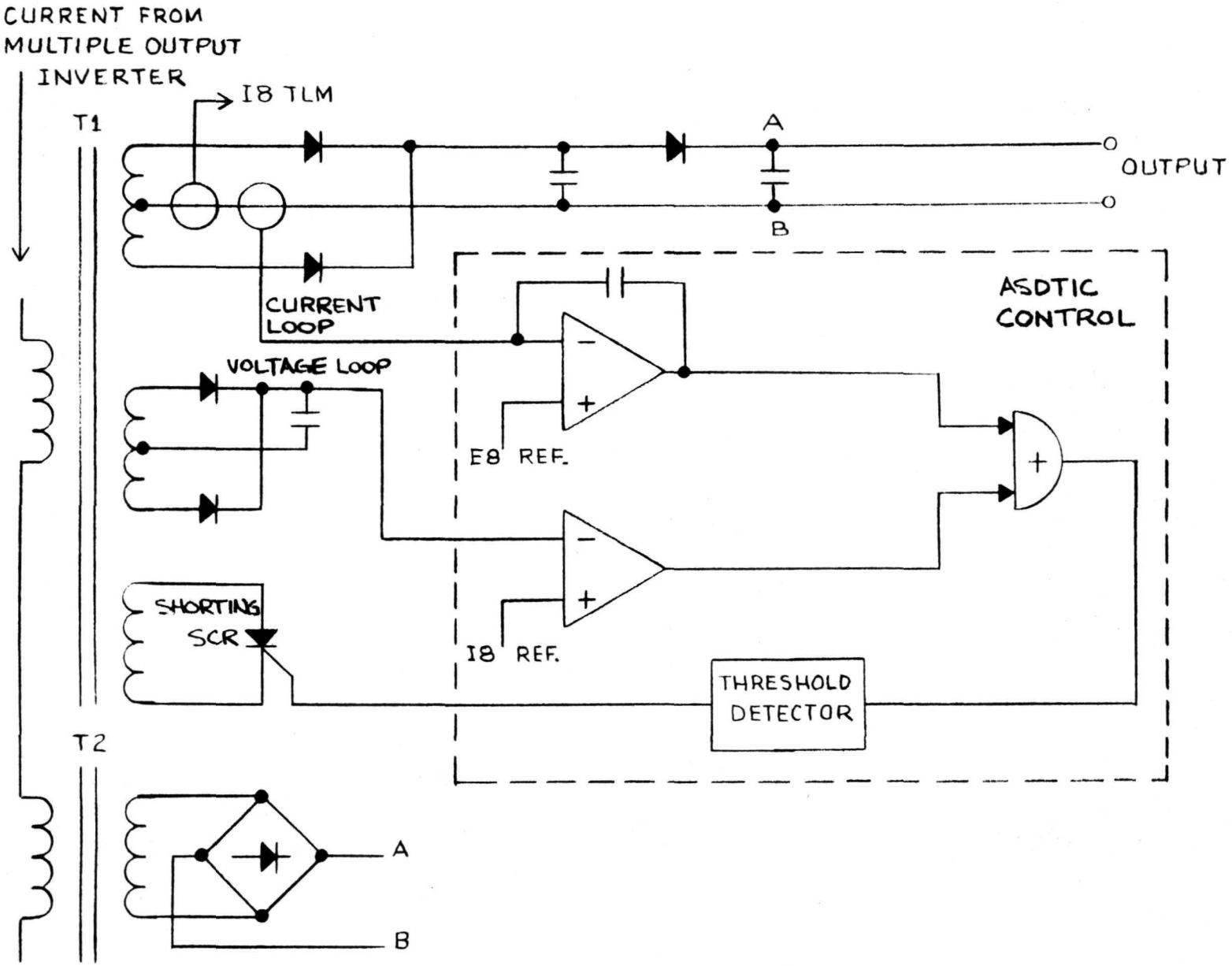


FIGURE 4-8 V8 - NEUTRALIZER KEEPER POWER SUPPLY BLOCK DIAGRAM

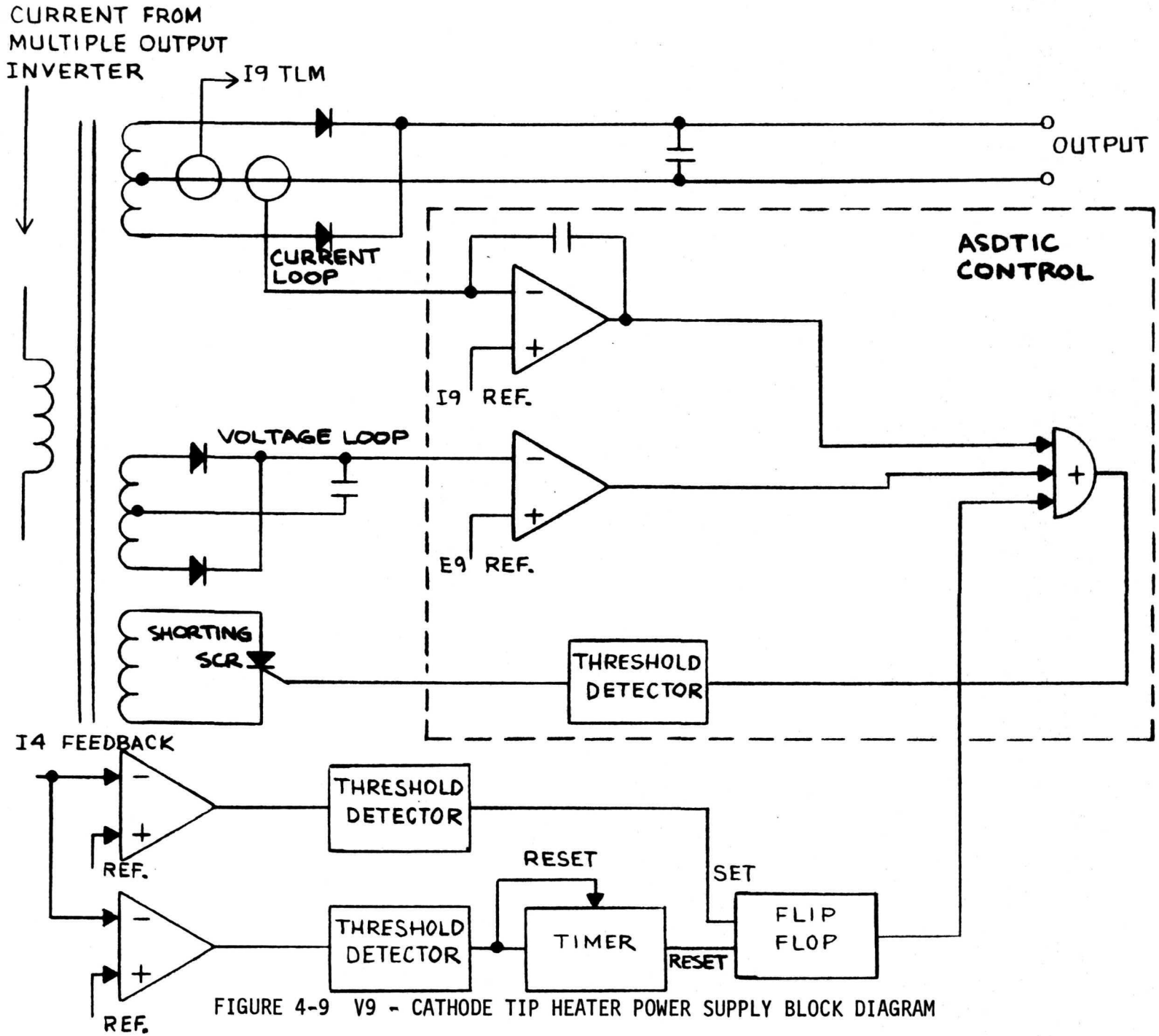


FIGURE 4-9 V9 - CATHODE TIP HEATER POWER SUPPLY BLOCK DIAGRAM

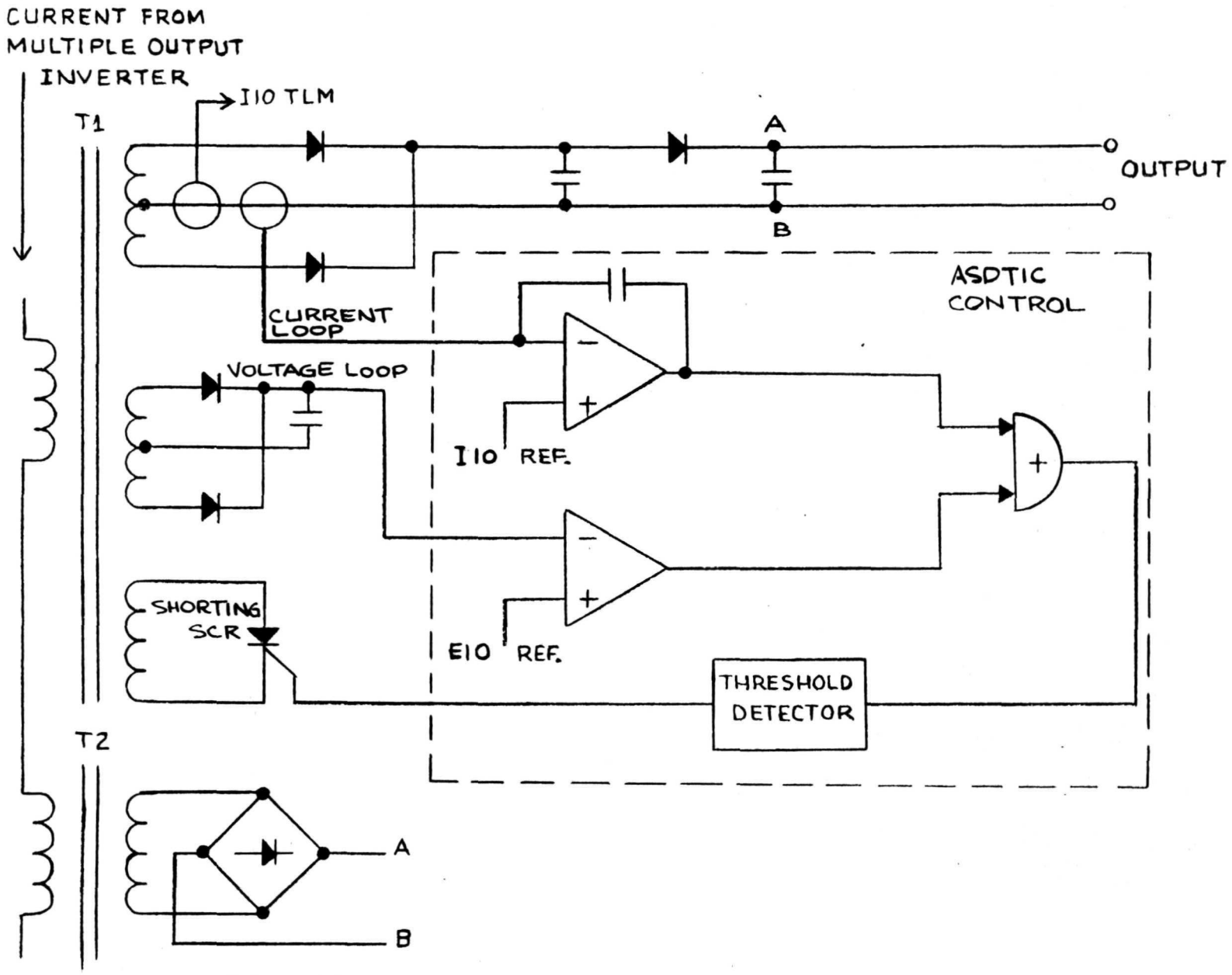


FIGURE 4-10 V10 - CATHODE KEEPER POWER SUPPLY BLOCK DIAGRAM

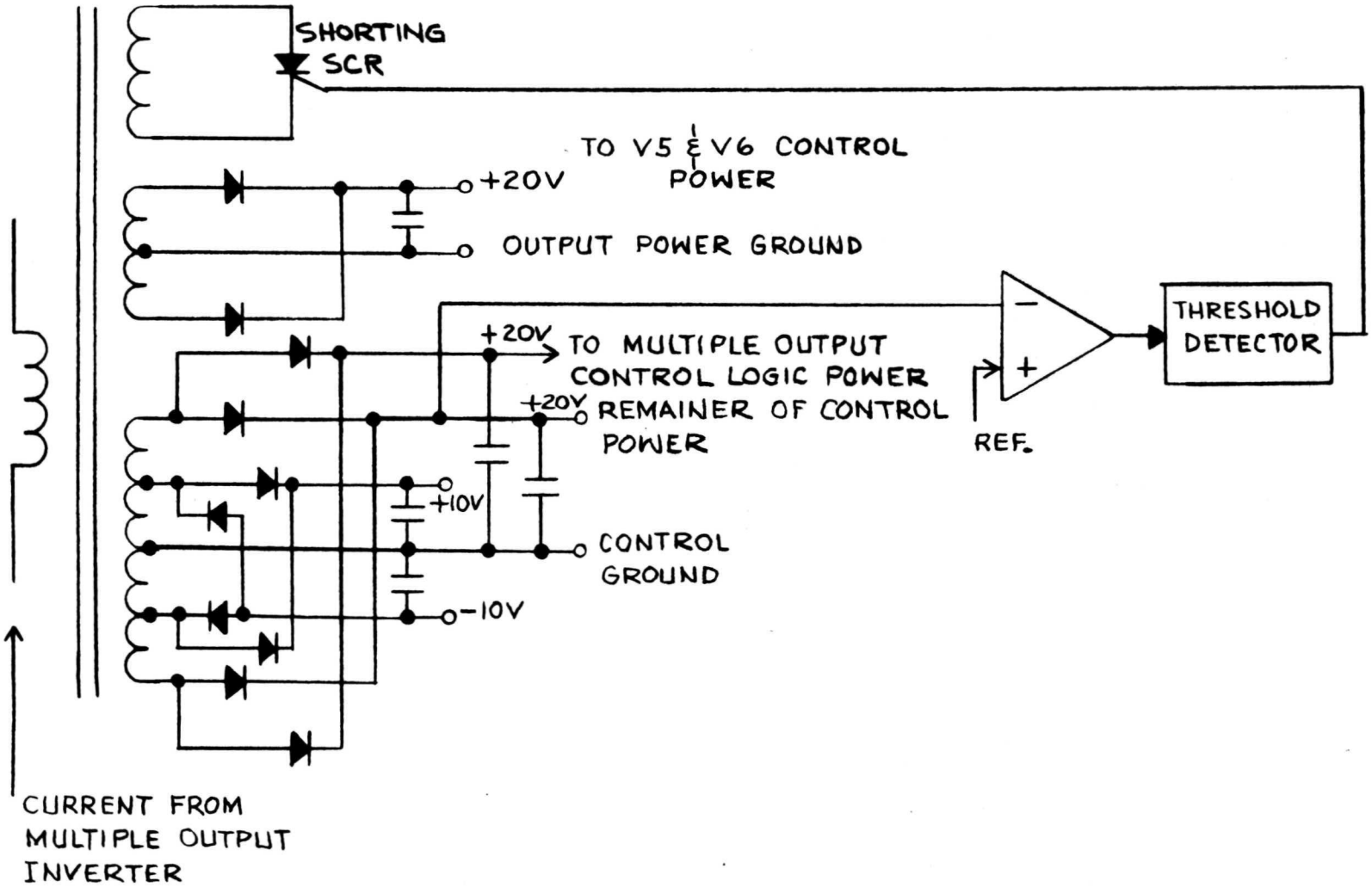


FIGURE 4-11 INTERNAL AUXILIARY POWER SUPPLY BLOCK DIAGRAM

4.3 Command and Protection System

The command and protection system logic block diagram has been completed, and Figures 4-12 through 4-14 show the detailed mechanization. Figure 4-12 shows the interface between the input commands and the different circuits in the power processor.

The ON-1 command is used to initiate the panel preheat. The ON-2 command is "and" gated with the panel $0^{o}F$ signal and starts the multiple output inverter, turns on the auxiliary dc source (Figure 4-14) to power the multiple output inverter control logic and starts the five minute engine preheat timer. The ON-3 command is "and" gated with the five minute timer output signal and allows the remainder of the outputs to turn on.

The OFF-1 command turns the V_2 supply off and enables the I_5 sensor to become active. When I_5 reads I_5 ref/2, an output signal turns the power processor off. The OFF-2 command is used for emergency turn off of the power processor. The undervoltage and overvoltage sensor on the input power bus can also turn the power processor off.

The I_5 reference command is amplified by a voltage follower amplifier to increase the loading impedance on the I_5 reference command source. The output is also sent to a function generator which generates the I_4 reference as a function of the I_5 reference command.

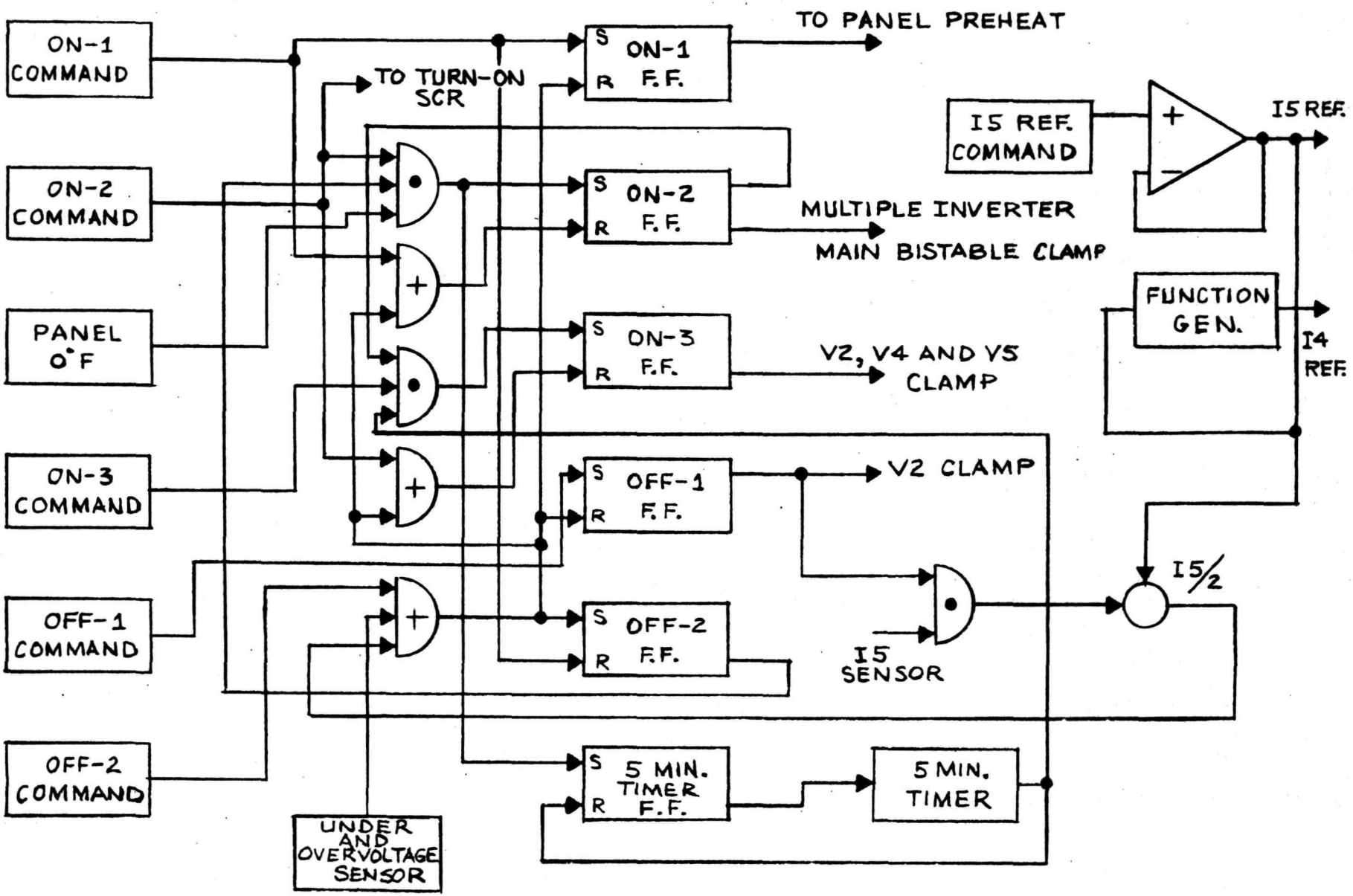


FIGURE 4-12 COMMAND SYSTEM BLOCK DIAGRAM

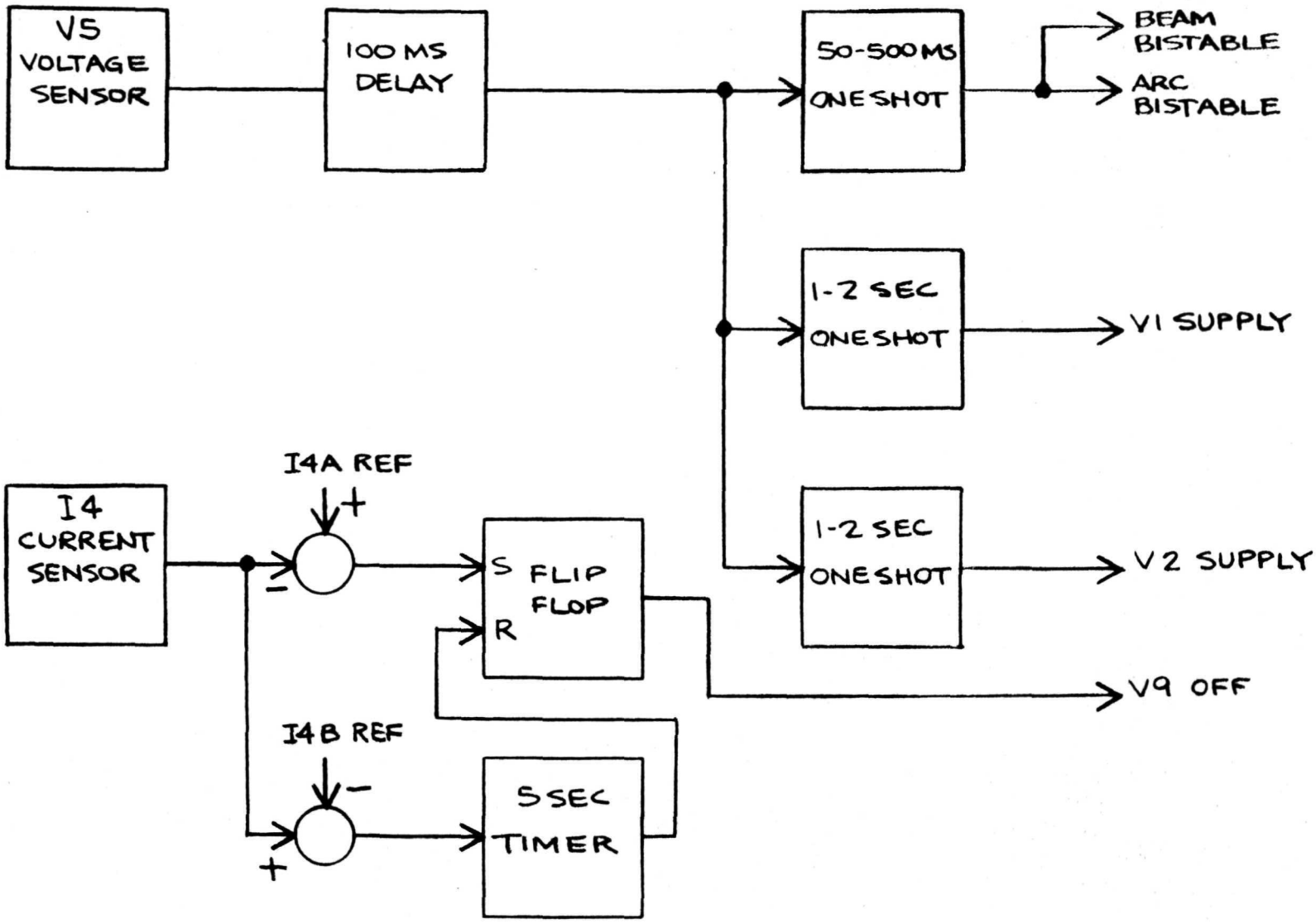


FIGURE 4-13 PROTECTION SYSTEM BLOCK DIAGRAM

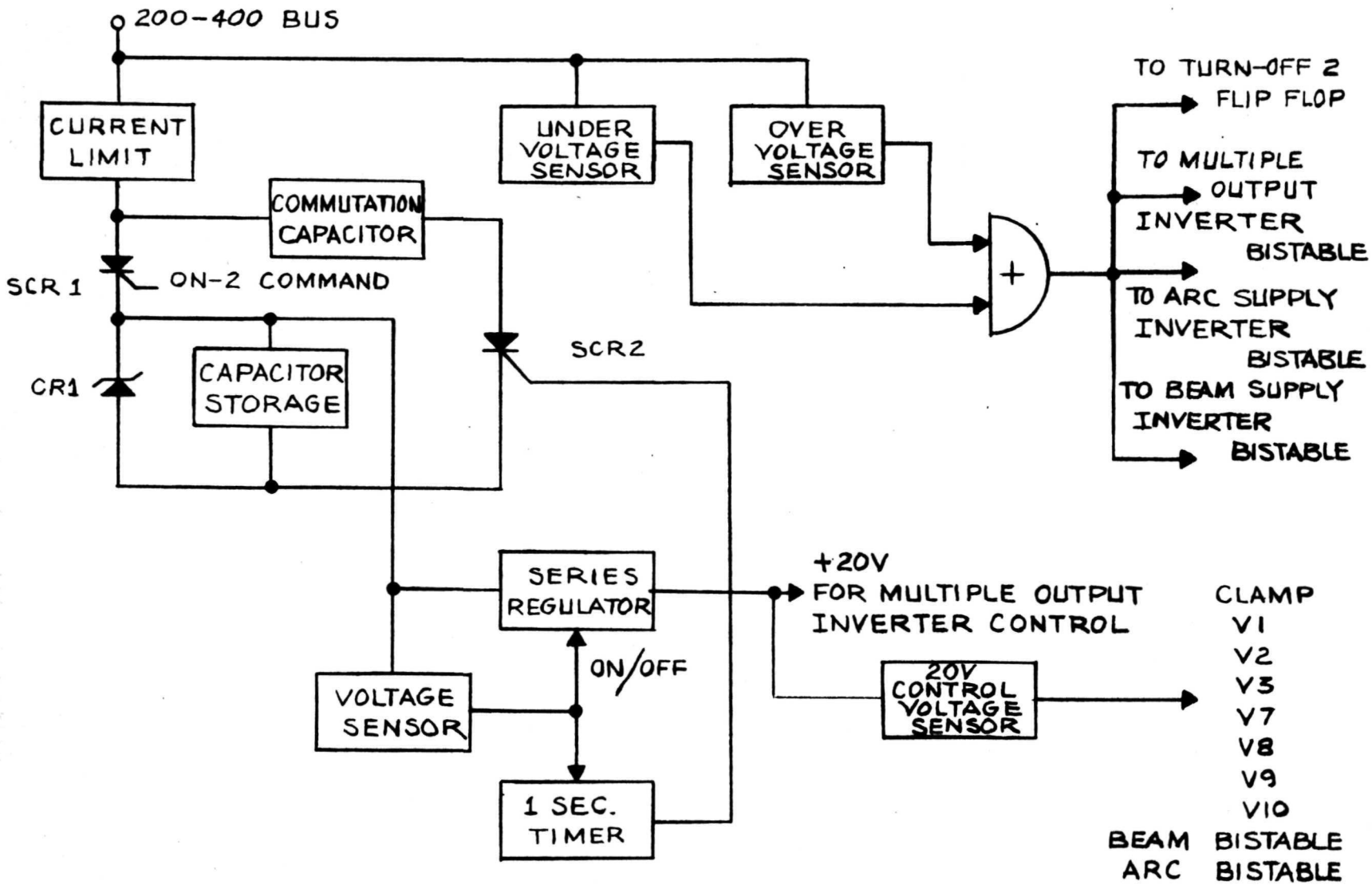


FIGURE 4-14 STARTUP/INPUT VOLTAGE PROTECTION BLOCK DIAGRAM

Figure 4-13 shows the protection of the engine due to overloads on the beam supply and automatic sequencing of the V_9 supply. If the V_5 (beam) supply is below 90% of rated value for 100 milliseconds, three one shots operate. The first one shot turns off the beam (V_5) and arc (V_4) supply inverters for an adjustable period. The second one shot turns off the magnet supply (V_1) and the third one shot turns off V_2 supply. All one shots have adjustable time periods.

I_4 sensor is compared to two different references. If I_4 becomes greater than I_4A reference, supply V_9 is turned off. If I_4 becomes less than I_4B reference, a five second timer becomes active and after the fixed period turns V_9 on again.

Figure 4-14 shows the startup and input voltage protection system for the power processor. The ON-2 command turns on SCR-1. DC current from the 200-400 V bus passes through a current limit and charges up the capacitor storage network. Zener diode CR1 limits the maximum voltage that can appear on the capacitor. A voltage sensor senses the voltage on the capacitor and when it reaches a fixed value, a series regulator turns on and passes current to the multiple output inverter control logic. A one second timer is also turned on which turns on SCR-2 and commutates SCR-1 off. If the voltage on the storage capacitor falls below a predimined value before the inverter can be started, the voltage sensor turns the series regulator off and the storage capacitor is allowed to recharge.

4.4 System Grounding Philosophy

Figure 4-15 details the grounding philosophy for the ion engine power processor. Two separate internal grounds are included in the power processor:

- Solar Array Ground/Control Circuit Ground
- Output Power Ground

Each ground can be connected to the power system common ground.

Control circuit grounds in series inverters No. 1, 2 and 3, all output regulator control circuit grounds except V_5 and V_6, and all command and telemetry signal grounds are tied to the control circuit ground.

The $V_{5\pm}$ V_6 regulator power ground is only connected to the beam and accelerator supplies and there is no connection to the control circuit ground. No overload current transient on the output can thus appear on the control circuit ground.

All commands and telemetry could be easily modified to be a separate ground except for the I_5 reference command which has to be common to the control circuit ground.

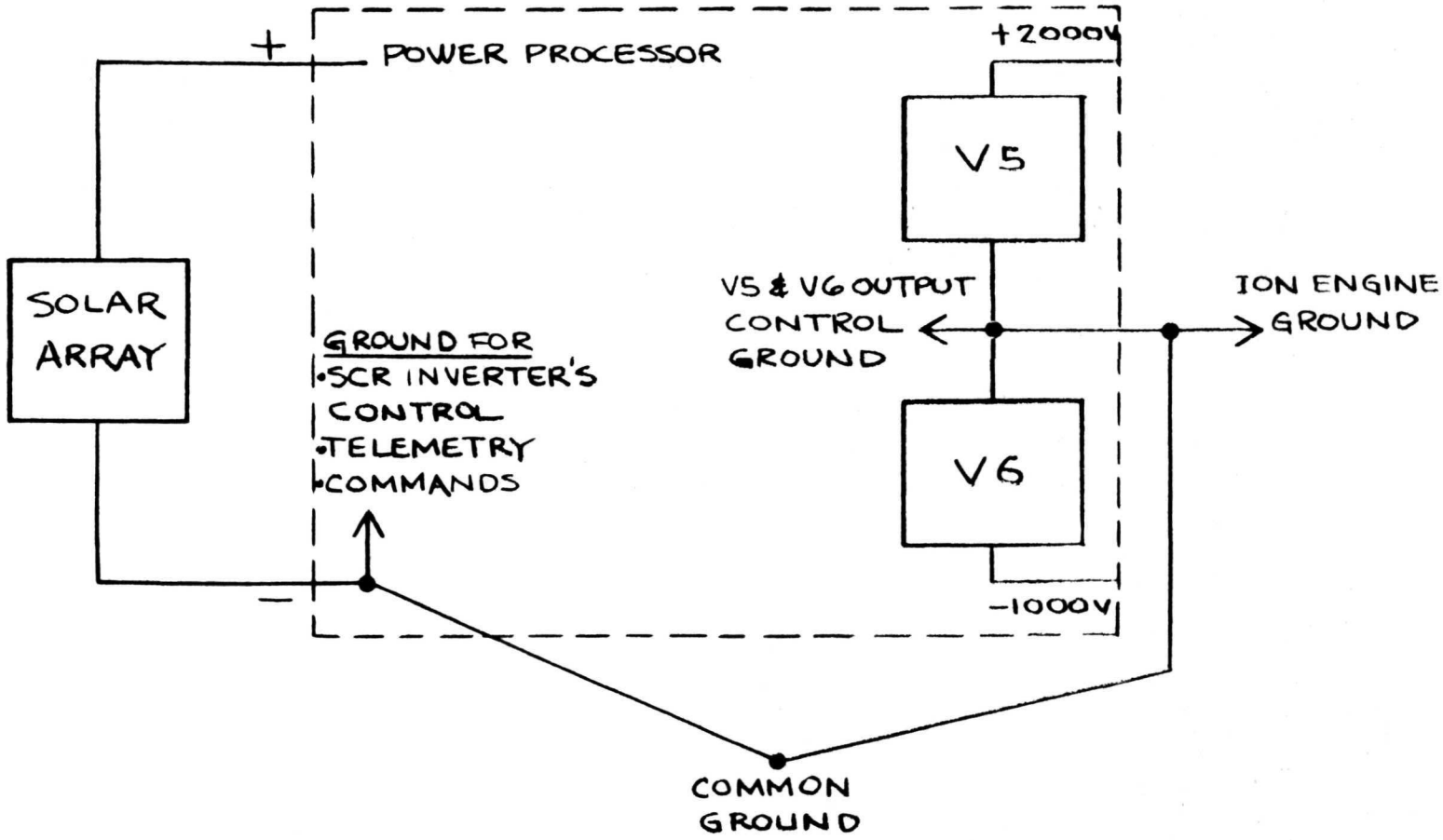


FIGURE 4-15 POWER PROCESSOR GROUNDING

5.0 ELECTRICAL DESIGN AND BREADBOARD TESTING

This section documents the baseline power processor electrical design details and the test data and identifies any particular design problems still outstanding.

5.1 Series Inverter Power Stage

5.1.1 Characteristics and Equations

The series controlled rectifier inverter utilizes a series L-C resonant circuit to provide the means of commutation of the inverter SCRs. Fig. 5-1A illustrates, in basic form, a push-pull configuration of this type of inverter. When one controlled rectifier is turned on, an oscillatory current flows through the series combination of the inductor L, the load transformer T, and the series capacitors C. The sinusoidal current flow, occuring at a frequency determined by the L-C components, is zero when an SCR is initially turned on, builds up to a maximum determined by the circuit parameters and then returns to zero. As the current passes through zero, the conducting SCR reverts to a non-conducting state.

To illustrate certain characteristics pecular to this type of inverter and to develop the basic equations of the series inverter the circuit of Fig. 5-1A has been redrawn, in Figure 5-1B to simplify the performance of a transient analysis. (In this circuit a switch is used to simulate the SCR.)

The current flowing through the inductor and transofrmer, i (t), upon closure of switch S1, is given by:

$$i\ (t) = \frac{E_{DO}-E_{TO}}{\sqrt{\frac{L}{2C}}}\ \text{SIN}\ \sqrt{\frac{1}{2LC}}\ t \qquad (1)$$

where E_{DO} is the voltage existing at the junction of the two capacitors at time t = 0 (the time of switch closure) and E_{TO} is the voltage appearing across the transformer primary. The latter voltage is clamped at a value established by the voltage appearing across the output capacitor, C_{out}.

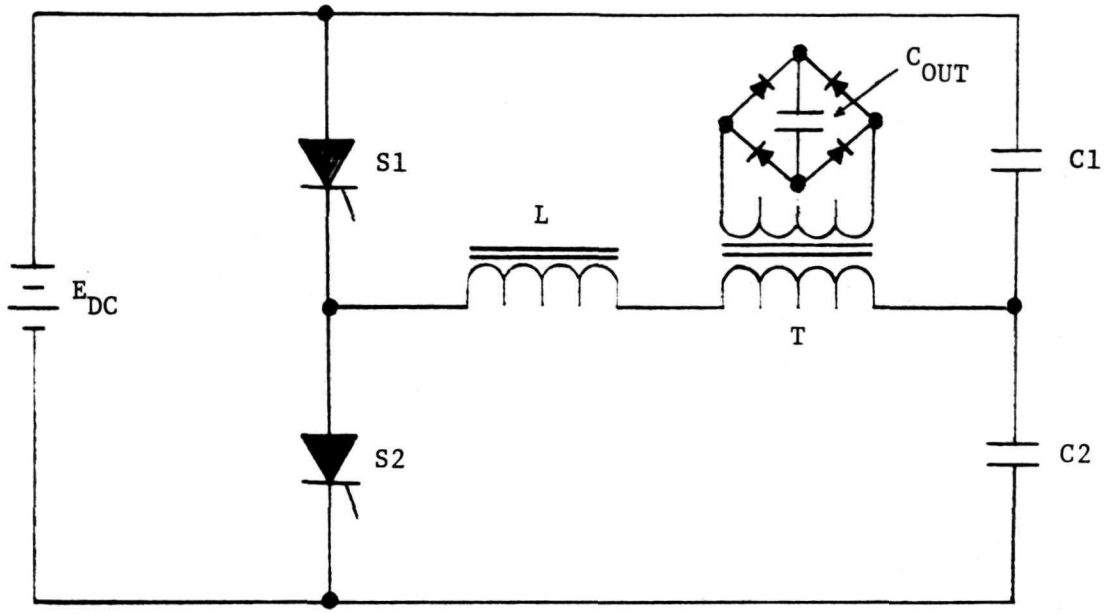


FIGURE 5-1A BASIC SERIES INVERTER

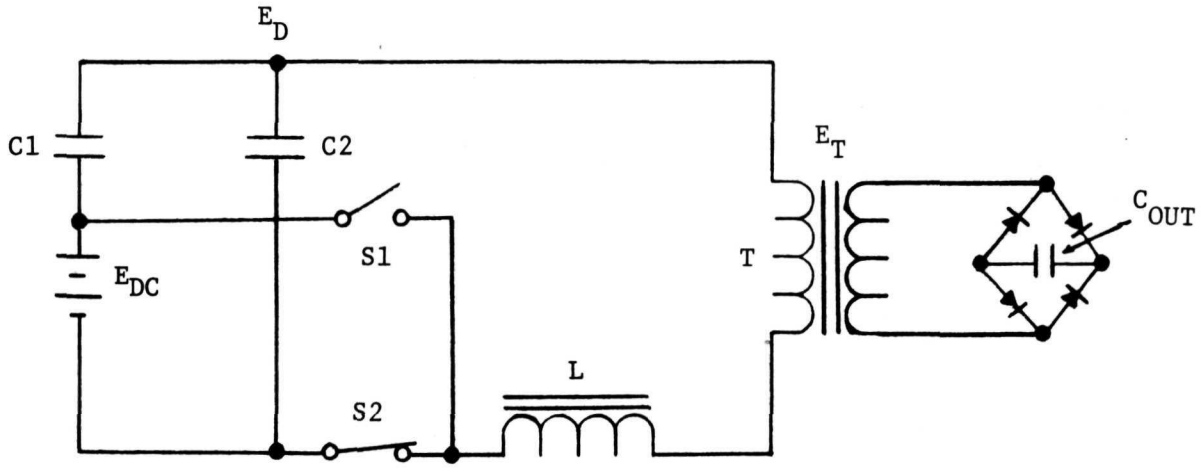


FIGURE 5-1B TRANSIENT NETWORK ANALYSIS

With the currents and voltages for each element established, the flow of energy from the power source to the load and capacitors, can be analysed. Expressing the energy balance in equation form results in

$$\Sigma_{source}\ (0\leq t\leq\tau) = \Delta\Sigma c\ (0\leq\ \leq\tau) + \Sigma_{L}\ (0\leq t\leq\tau) + \Sigma_{loss}\ (0\leq t\leq\tau) \qquad (7)$$

which shows that source energy over a single switching event consists of energy delivered to the load, (Σ_L), that delivered to circuit loss elements, Σ_{loss}, and a surplus amount which is stored in the previously charged series capacitors, $\Delta\Sigma c$. If an energy surplus continues to be supplied during succeeding switching events, the total energy stored in the capacitor will increase and eventually become infinite. Means, therefore, must be provided to limit the capacitor energy build-up so that components will be operated safely within their ratings.

Figures 5-1C(a) through 5-1C(d), illustrate the fast build-up of energy in the series capacitors under the conditions of output short circuit and system turn-on (output capacitors fully discharged). During normal steady-state operation the build-up of capacitor energy still occurs but at a slower rate.

In Figure 5-1C(a), both series capacitors are charged to one half the value of the source voltage (100Vdc in the example shown) just prior to closure of switch S_2. When S_2 is closed, voltage is developed across the inductor and at the end of the half-period of the sinusoidal current flow, S_2 is opened and the capacitors voltages shown in Figure 5-1C(b) exist.

Figure 5-1C(c) shows the situation just prior to closure of switch S_1. The driving source voltage is now 300V and the peak current flow through S_1 and the inductor is three times the value obtained in the previous half-cycle. Figure 5-1C(d) shows the capacitor voltages existing at the end of the second half-cycle. These voltages which initially were 100V each, have, in the course of two power pulses, changed to 300V and 500V, respectively. Thus it is seen how quickly an intolerable build-up can occur.

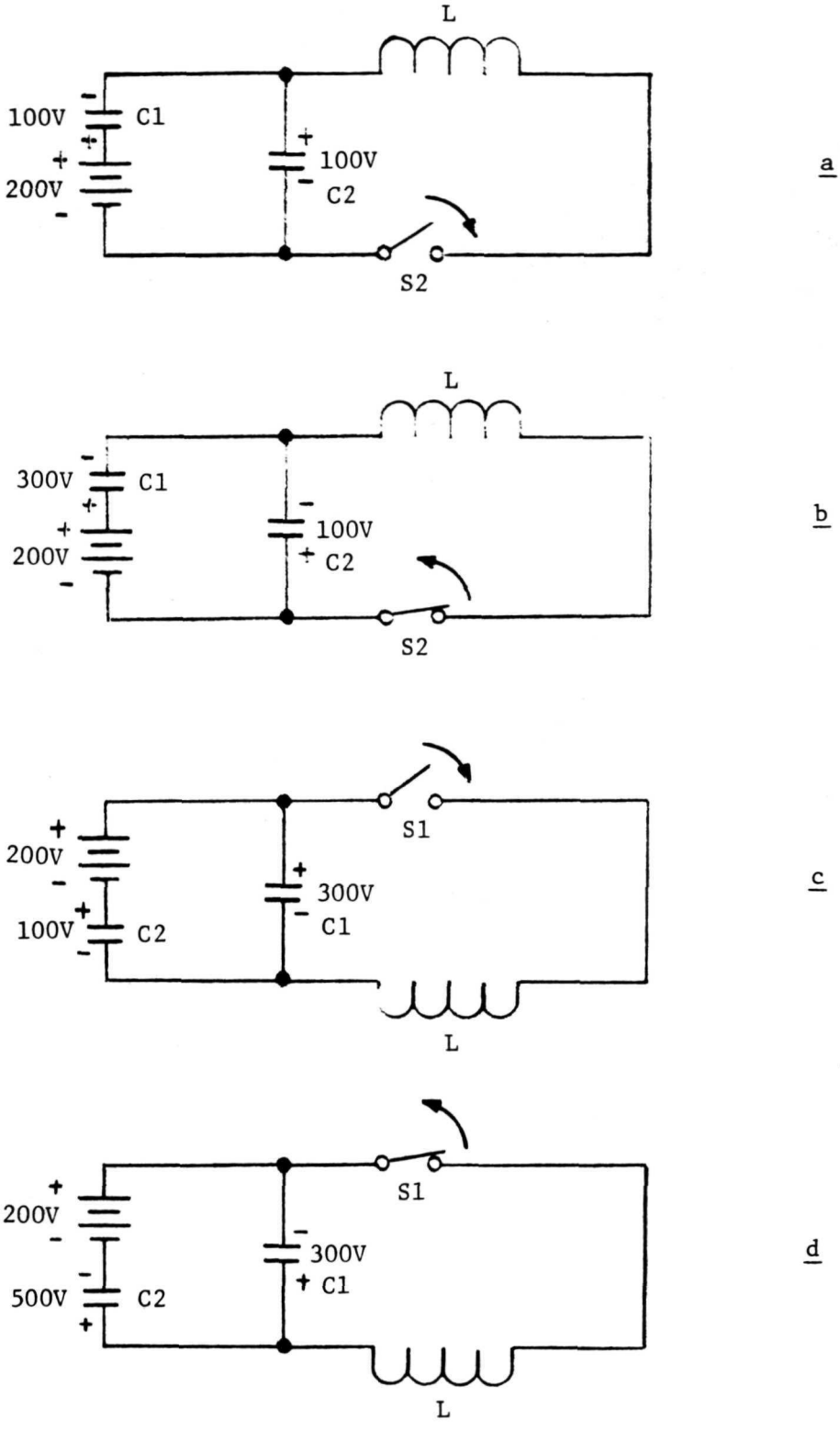


FIGURE 5-1C ENERGY BUILDUP OF SERIES INVERTER

This analysis assumes that no resistive components exist in C, L, T and the source, E_{DC}, presence of which would only slightly modify the results of the analysis.

The current through each series capacitor is i/2 and as a consequence, the current through the power source, E_{DC}, is also i/2. The peak energy sustained by the inductor L, needed for design, is given by:

$$\Sigma L = \frac{1}{2} L I_P^2 \tag{2}$$

where I_P is the peak value of i (t) and ΣL is the inductor energy. The inductor voltage, V_L, is obtained from

$$V_L = L \frac{di}{dt} \tag{3}$$

Substituting Equation (1) into Equation (3) gives

$$V_L = (E_{DO}-E_{TO}) \cos \sqrt{\frac{1}{2LC}}\, t \tag{4}$$

The voltage across each capacitor C, can be determined from

$$Vc = Vo_x + \frac{1}{c} \int \frac{i}{2}\, dt \tag{5}$$

where Vo_x is the initial voltage on the capacitor under consideration. Substituting Equation (1) into Equation (5), Vc can be rewritten as

$$Vc = Vo_x-(E_{DO}-E_{TO}) \cos \sqrt{\frac{1}{2LC}}\, t \tag{6}$$

The transient analysis can be extended to describe circuit operation with either step changes in transformer load voltage, such as would occur under short circuit conditions or transformer saturation, or with step changes in the source voltage, E_{DC}.

There are two basic methods for limiting the capacitor build-up:

a) Transfer of the stored energy in the inductor to the load or to the source at a point during the half-cycle when a particular capacitor voltage level has been reached.

b) Transfer of the excess energy stored in the capacitor to the load or to the source between the end of a half-cycle power pulse and the start of the following pulse.

In the succeeding paragraph, details on the particular system used for this application is described.

5.1.2 Method of Limiting Energy Build-up in the Series Inverter

The basic schematic of the series resonant inverter power stage is shown in Figure 5-1D.

Its operation can be described as follows:

SCR's 1 and 2 are the main power switches and SCR's 3 and 4 are the auxiliary power switches. When SCR-1 is turned on, current flows through inductor L1 & L2, output transformer T2, and series capacitor C1 and C2. The voltage across capacitor C2 is monitored and when a predetermined maximum is reached, auxiliary SCR-3 is fired. This allows current to continue to flow through L1, L2 and T2 until all the energy sotred in L1 & L2 is reduced to zero. With the firing of SCR-3, SCR-1 is allowed to turn-off as a result of a reverse bias voltage derived from the voltage across C2. When the current in SCR-3 linearly decays to zero, it turns off, completing one switching event.

The current sensors (T1) were originally in series with output transformer T2 next to the center connection between the two series capacitors C1 & C2. In the event that apreviously conducting auxiliary SCR reignited after another cycle began the current sensors could not determine this event and a system would not be protected from excessive energy. Moving the current sensors in series with each resonant inductor L1 & L3 always detected a false current flow in the auxiliary SCR and protected the system.

The center tap inductor L2 was added to ensure that when a new half cycle began that the previous conducting auxiliary SCR would be back biased by the induced voltage from the other half of inductor L2 and prevent any reignition.

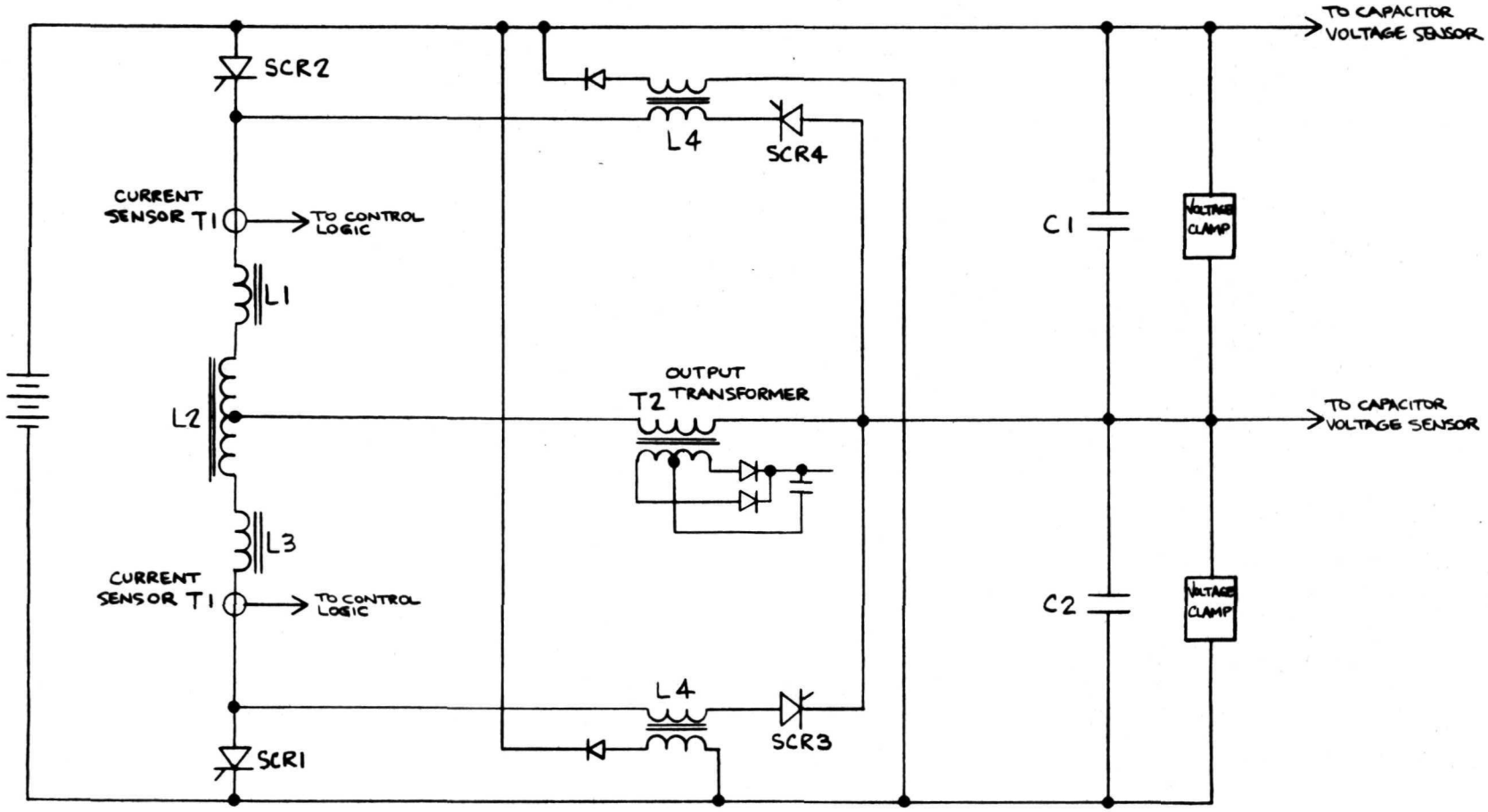


FIGURE 5-1D BASIC SCHEMATIC OF SERIES RESONANT INVERTER POWER STAGE

The capacitor voltage clamp circuit would sense that the SCR control logic had malfunctioned and allowed the capacitor voltage to overshoot. The voltage clamp circuit would bleed off excess energy and the next half cycle, the SCR control logic would take over control again.

The center tap inductor L2 and the capacitor voltage clamp are back-up protection for the SCR control logic in the event there was a malfunction.

Inductor L4 was added to reduce the switching losses in the main line SCR and auxiliary SCR when the auxiliary SCR was turned on. The inductor absorbs voltage during the turn-on. During the turn-off of the main line SCR high reverse current flows through the SCR and when it turns off the high amp-turns (energy) in the inductor flows in the secondary wind on L4 through the diode back into the source. The addition of this inductor and diode improved the inverter efficiency approximately 0.75%. The inductance value had to be carefully selected so as not to interfere with the protection function of the auxiliary SCR and allow the series capacitor C1 & C2 voltage to overshoot.

5.2 SERIES RESONANT INVERTER CONTROLS

The logic block diagram for the SCR series resonant inverter control logic is shown in Figure 5-2. It shows the main bistable commanding the firing of the main line SCR's as a function of the various inputs. The main bistable also controls the transformer bias driver which continues the excitation of the power transformer after the end of a half cycle to eliminate power transformer saturation during the next half cycle. The half cycle includes the time period when the main and auxiliary SCR's are conducting power to the power transformer and the time period when the system is kept off due to an intentional delay of 10 microsecond or longer due to the output regulator or the miller integrator.

Two current sensors are used to sense when either the positive or the negative half cycle current goes to zero and operate the respective 10 microsecond monostables, and transfer the local bistable. If the signals from the miller integrator and the output regulator are correct, the main bistable is allowed to transfer.

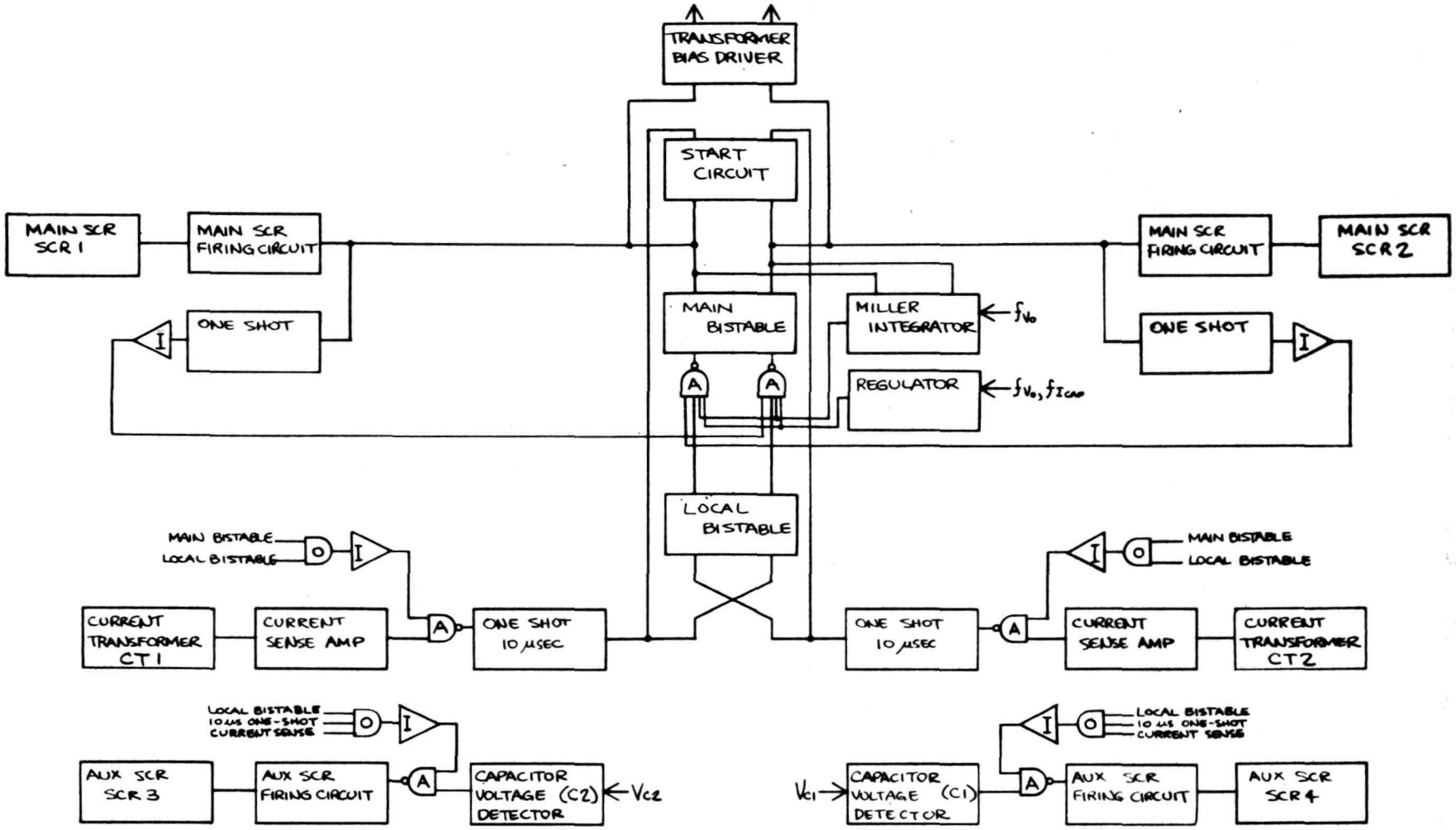


FIGURE 5-2 SERIES RESONANT INVERTER CONTROL LOGIC BLOCK DIAGRAM

The miller integrator is used to give a soft start and to balance the time period for the two half cycles during startup to eliminate power transformer saturation.

The start circuit is a low frequency oscillator which transfers the local bistable. When the system is running at normal frequencies, the output from the main bistable clamps the start circuit.

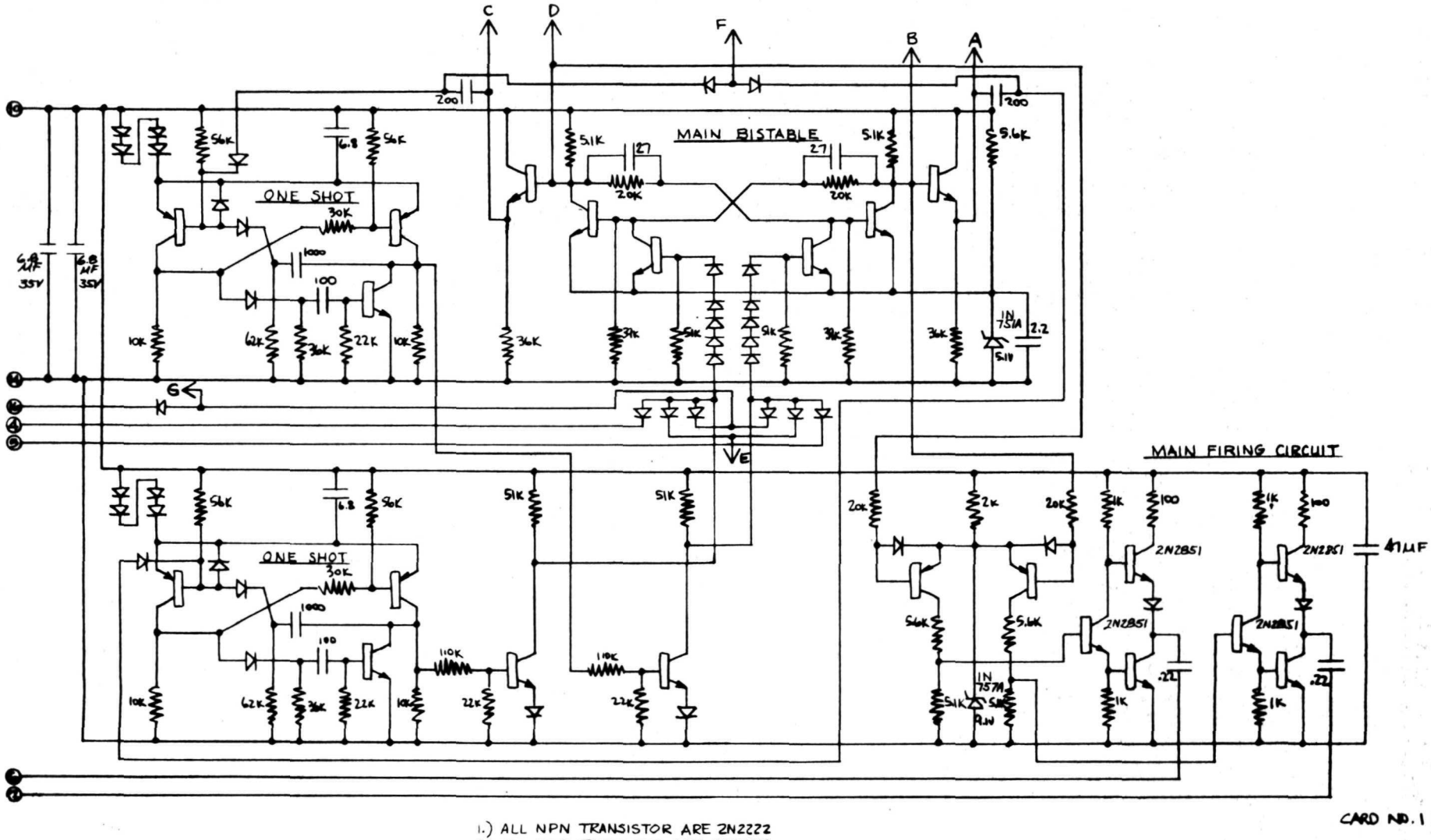
The capacitor voltage sensor senses the voltages on the two series capacitors and when a capacitor voltage reaches 450 volts, the respective auxiliary SCR is fired and stops amy additional current flow into the capacitor. Clamping circuits are added to allow the auxiliary SCR's to be fired only during its correct firing event.

The schematics of the SCR inverter control logic circuit of the series inverter are shown in Figures 5.3 through 5-7. The schematics represent the circuitry that was used in the three Series Resonant Inverters.

The inverter control logic was contained in four common control cards with an additional control card which includes the output regulator controls. Card 1 (Figure 5-6A and B) includes the main bistable, the SCR firing circuit, the start circuit, the miller integrator and the output regulator (which is normally not used)but only when integrating the output regulator card. Card 2 (Figure 5-7A and B) includes the local bistable, the 10 microsecond one shot and the transformer bias driver circuit Card 3 (Figure 5-8) includes the capacitor sensors and the auxiliary SCR firing circuits. Card 4 (Figure 5-9) includes the current sensor circuit. Figure 5-10 shows the interconnected between the cards and the power inverter circuit.

The problem areas originally associated with the series inverter control logic circuit have been satisfactorily remedied and the changes have been incorporated in the breadboard. The problem areas were the following:

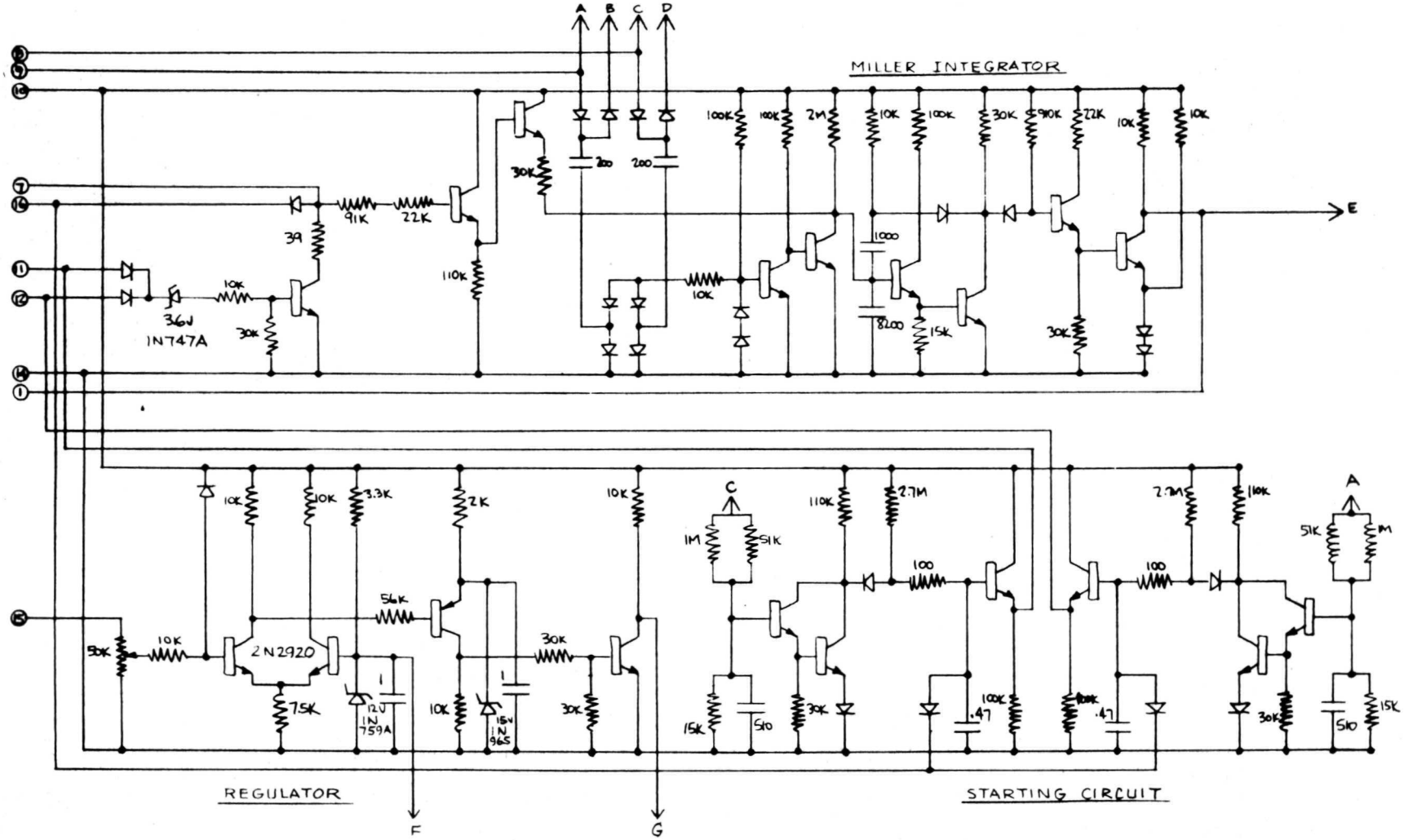
- Current Sensor
- Voltage Sensor



1.) ALL NPN TRANSISTOR ARE 2N2222
2.) ALL PNP TRANSISTOR ARE 2N2907A
3) ALL DIODES ARE IN3600

NOTES: UNLESS OTHERWISE SPECIFIED

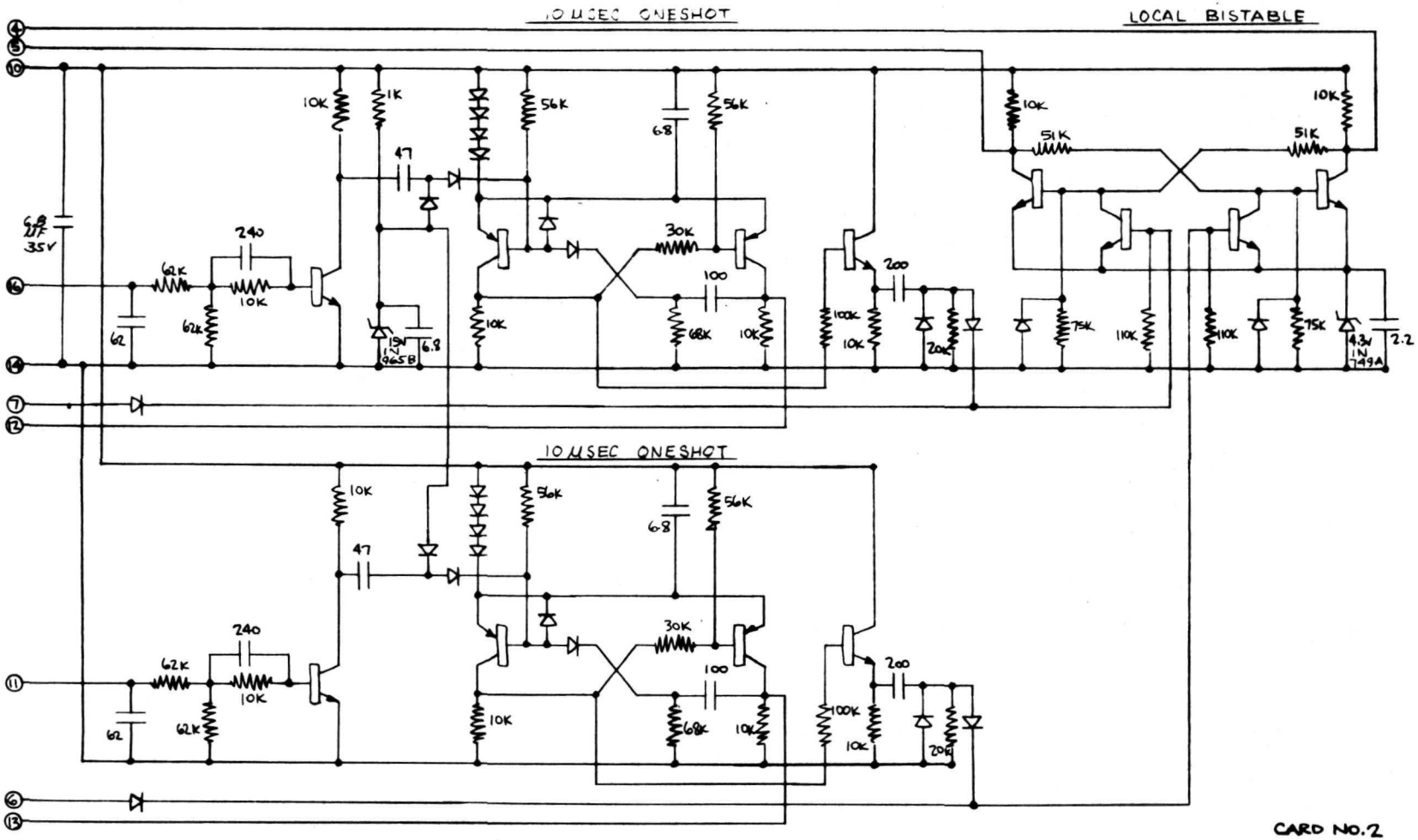
FIGURE 5-3A SCHEMATIC OF SERIES RESONANT INVERTER CONTROL LOGIC
Main Bistable and Main SCR Firing Circuit



1.) ALL NPN TRANSISTOR ARE 2N2222
2.) ALL PNP TRANSISTOR ARE 2N2907A
3.) ALL DIODES ARE 1N3600

NOTES: UNLESS OTHERWISE SPECIFIED

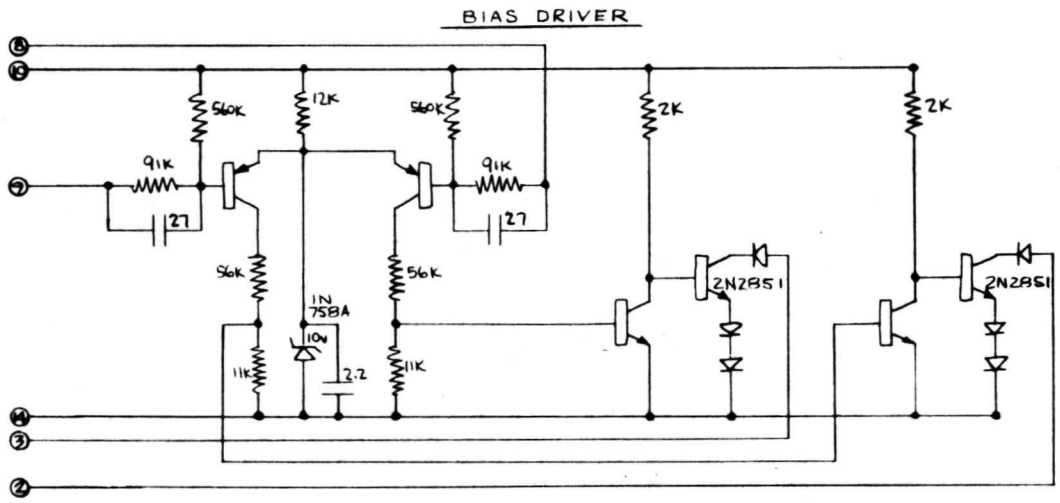
FIGURE 5-3B SCHEMATIC OF SERIES RESONANT INVERTER CONTROL LOGIC
Miller Integrator, Regulator and Start Circuit



1.) ALL NPN TRANSISTOR ARE 2N2222
2.) ALL PNP TRANSISTOR ARE 2N2907A
3.) ALL DIODES ARE IN3600

NOTES: UNLESS OTHERWISE SPECIFIED

FIGURE 5-4A SCHEMATIC OF SERIES RESONANT INVERTER CONTROL LOGIC
10 usec One-Shot and Local Bistable

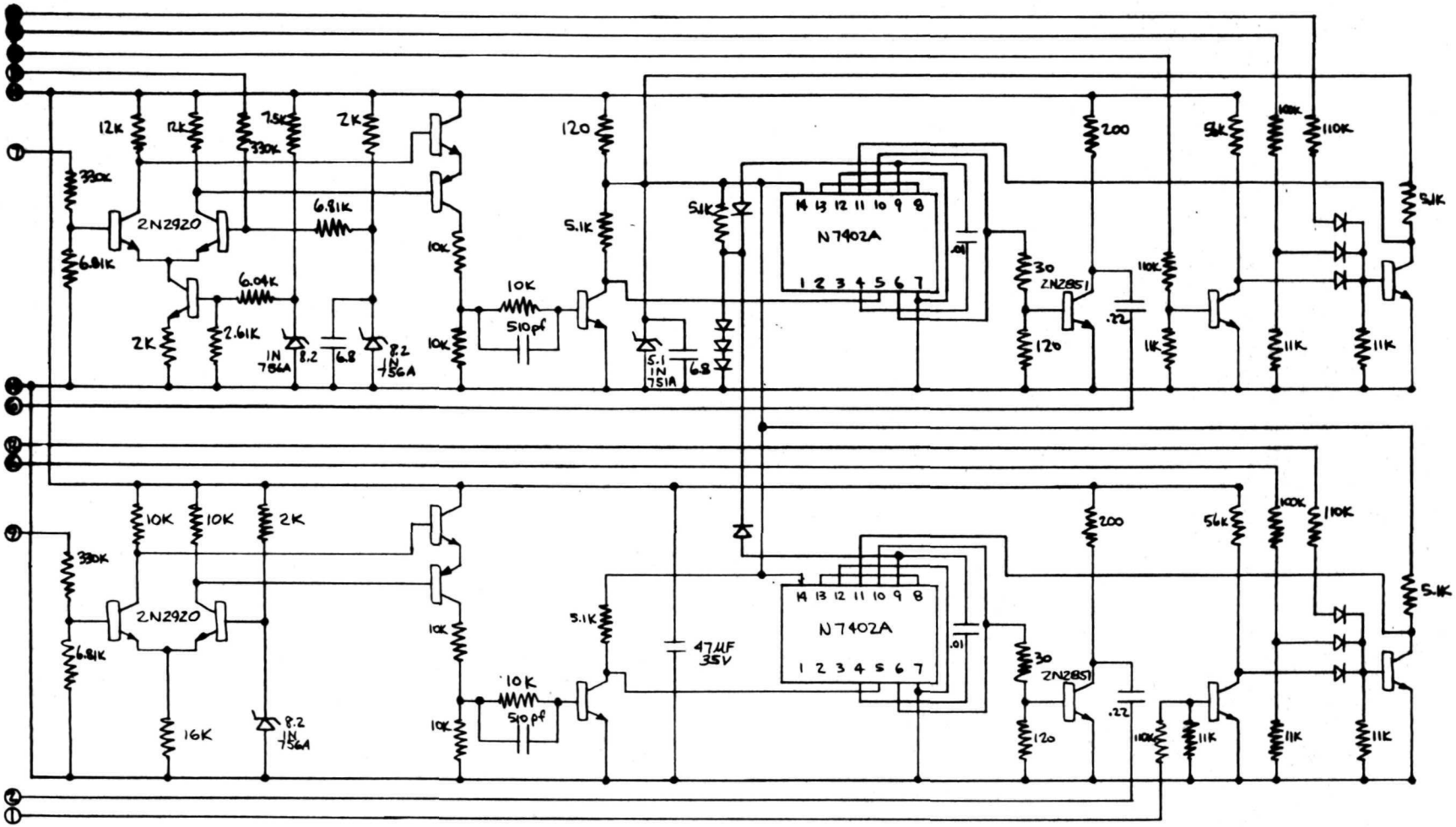


1.) ALL NPN TRANSISTOR ARE 2N2222
2.) ALL PNP TRANSISTOR ARE 2N2907A
3.) ALL DIODES ARE IN3600

CARD NO. 2

NOTES: UNLESS OTHERWISE SPECIFIED

FIGURE 5-4B SCHEMATIC OF SERIES RESONANT INVERTER CONTROL LOGIC
Bias Driver

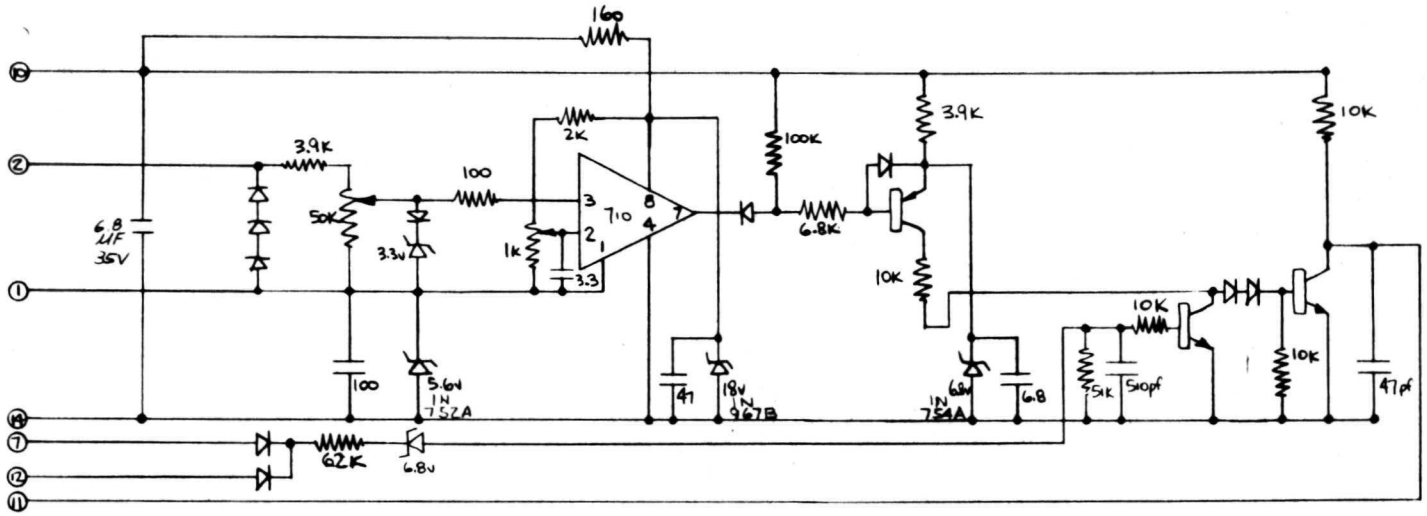


CARD NO. 3

1.) ALL NPN TRANSISTOR ARE 2N2222
2.) ALL PNP TRANSISTOR ARE 2N2907A
3.) ALL DIODES ARE IN3600

NOTES: UNLESS OTHERWISE SPECIFIED

FIGURE 5-5 SCHEMATIC OF SERIES RESONANT INVERTER CONTROL LOGIC
Capacitor Voltage Sensor and
Auxiliary Firing Circuit



1.) ALL NPN TRANSISTOR ARE 2N2222
2.) ALL PNP TRANSISTOR ARE 2N2907A
3.) ALL DIODES ARE IN3600

NOTES: UNLESS OTHERWISE SPECIFIED

FIGURE 5-6 SCHEMATIC OF SERIES RESONANT INVERTER CONTROL LOGIC Current Sensor

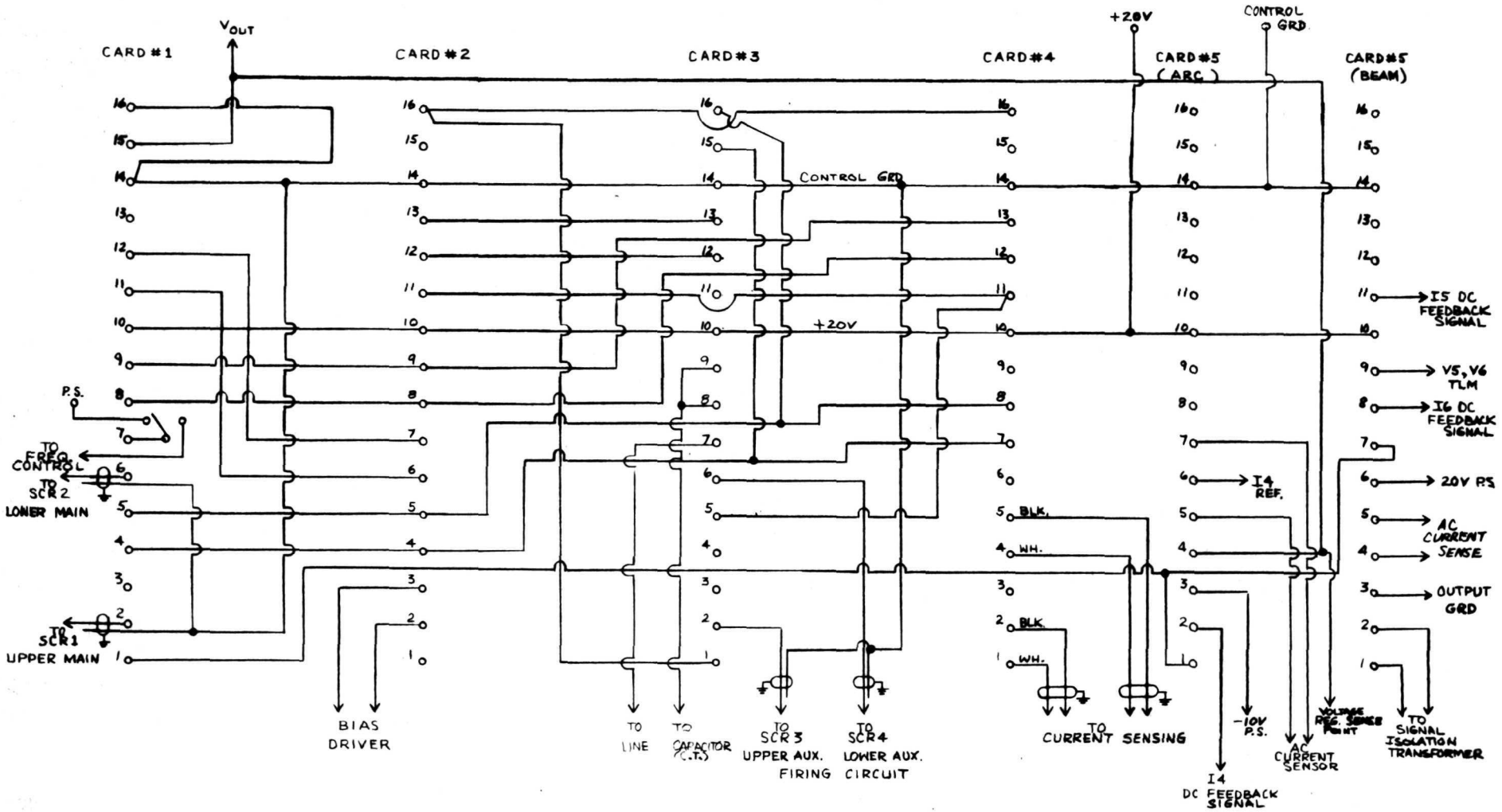


FIGURE 5-7 CONTROL CARD WIRING DIAGRAM

The current sensor circuit Fig. 5-9 as was previously implemented was susceptible to noise due to the fact that the clamp signals coming from the main and the local bistable were operating into a high impedance resulting in noise misfiring the current sensor. The change as shown in Fig. 5-9 clamps the base of the output transistor to ground which eliminates the noise problem.

Another problem associated with the current sensor circuit was the inability to set the threshold level of the sensor to obtain an output pulse less than 10μs wide under all operating conditions of the inverter. Since the current sensor transformer puts out a signal which is proportional to the rate of change of current, under short circuit conditions the rate of change of current is very small resulting in a low transformer output. If the current sensor threshold is set to detect the current sensor transformer output under short circuit conditions, then under normal operating conditions the curent sensor transformer output is very large and the output pulse width out of the current sensor circuit is wider than 10μs resulting in the limiting of the inverter power since initiation of a new cycle occurs at the trailing edge of the current sensor output pulse as shown in Fig. 5-11.

In order to overcome the problem of the total "OFF" time varying with the current sense transformer output, the triggering of the time delay multivibrator was changed from the trailing edge of the current sensor output pulse to the leading edge. The circuitry for this change is shown in Fig. 5-6. It consists of a transistor and resistors to invert the current sensor output signal. With this configuration, the minimum total "OFF' time of the inverter is controlled by the time-delay setting of the multivibrator and is independent of the current sensor output pulse width as shown in Fig. 5-9.

The capacitor voltage sensor was modified to decrease the delays in turning on the auxiliary SCR's. A major portion of the delay was occurring between the differential amplifier detector and the 7402A driver. Circuitry shown in Fig. 5-5, consisting of a NPN-PNP pair from the collectors of the differential amplifier and the addition of the R-C speed-up circuit in the base of the transistor driving the 7402A, resulted in eliminating most of the delay. The auxiliary SCR delay was reduced from 7 μsec to 1.5 μsec with these changes. The capacitor voltage overshoot is now limited to approximately 500V.

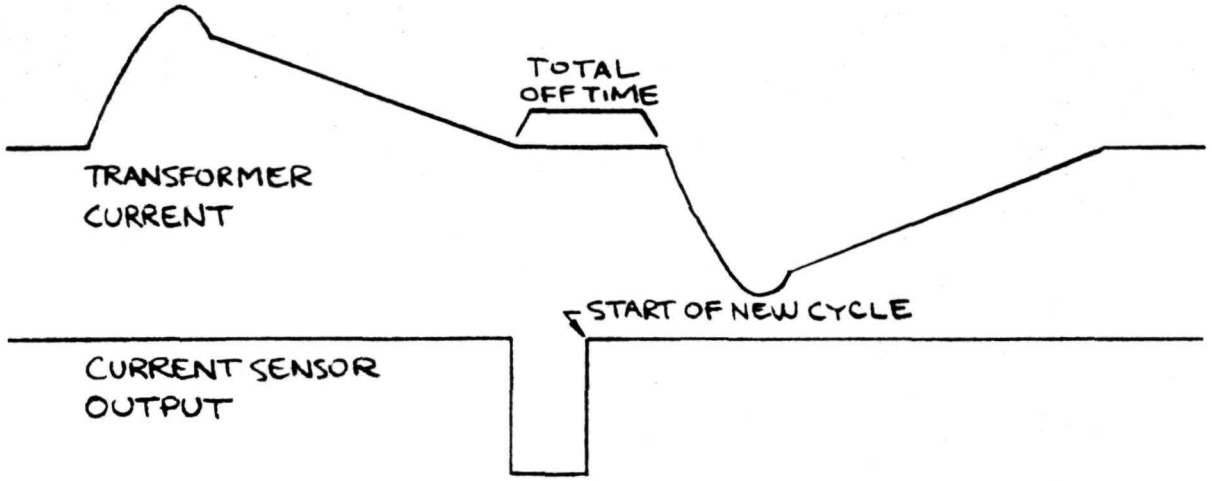


FIGURE 5-8 CURRENT SENSOR OUTPUT SIGNAL SENSING ON TRAILING EDGE

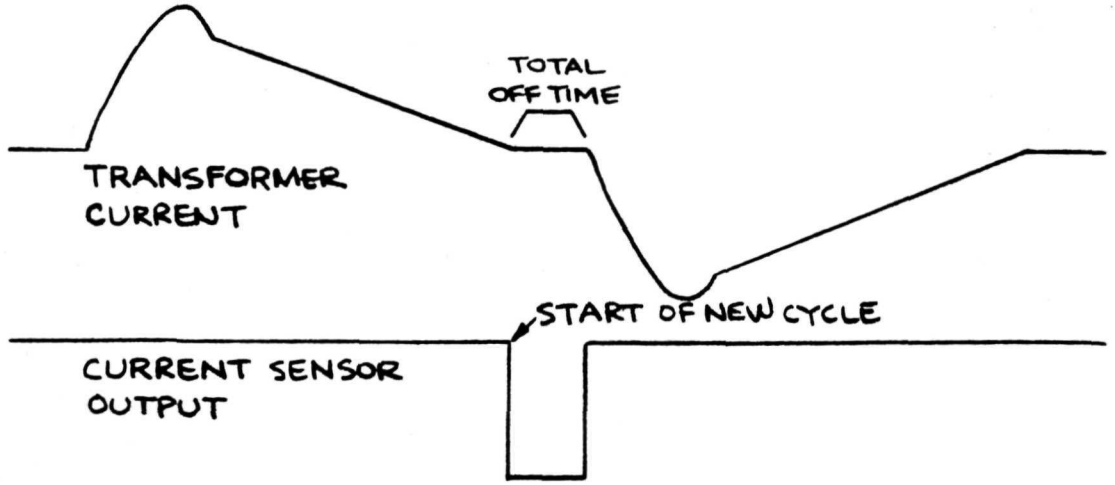


FIGURE 5-9 CURRENT SENSOR OUTPUT SIGNAL SENSING ON LEADING EDGE

5.3 Beam and Accelerator Supply (V5 and V6)

Figure 5-10 illustrates the schematic of the power circuit including the series resonant inductors and capacitors, the main line and auxiliary SCR's and their firing circuits, the output power circuitry and the capacitor voltage clamp circuit. The schematic of the control logic is shown in Figures 5-3 through 5.7.

The final configuration of the regulator using the ASDTIC concept has been incorporated into the beam supply breadboard. The control amplifier schematic is shown in Figure 5-11. Two regulating loops are incorporated.

- V5 Output regulation
- I6 Overload control

The V5 voltage regulation loop incorporates the ASDTIC amplifier which has a major and a minor feedback loop. In the major feedback loop, the output voltage is sensed, in the minor loop, capacitor AC current is sensed. The two signals are combined and fed to a threshold detector and then to an isolation transformer which provides isolation between input and output.

The I6 overload loop limits the current supplied from the V6 output.

Beam supply circuit waveform photographs for the main line and auxiliary SCR voltage and current are presented in Figures 5-12.

Figure 5-13 shows the instantaneous plot power in the main line and auxiliary SCR as a function of time. It shows the higher power dissipation that occurs when the auxiliary SCR is fired to limit the energy build up in the series capacitors.

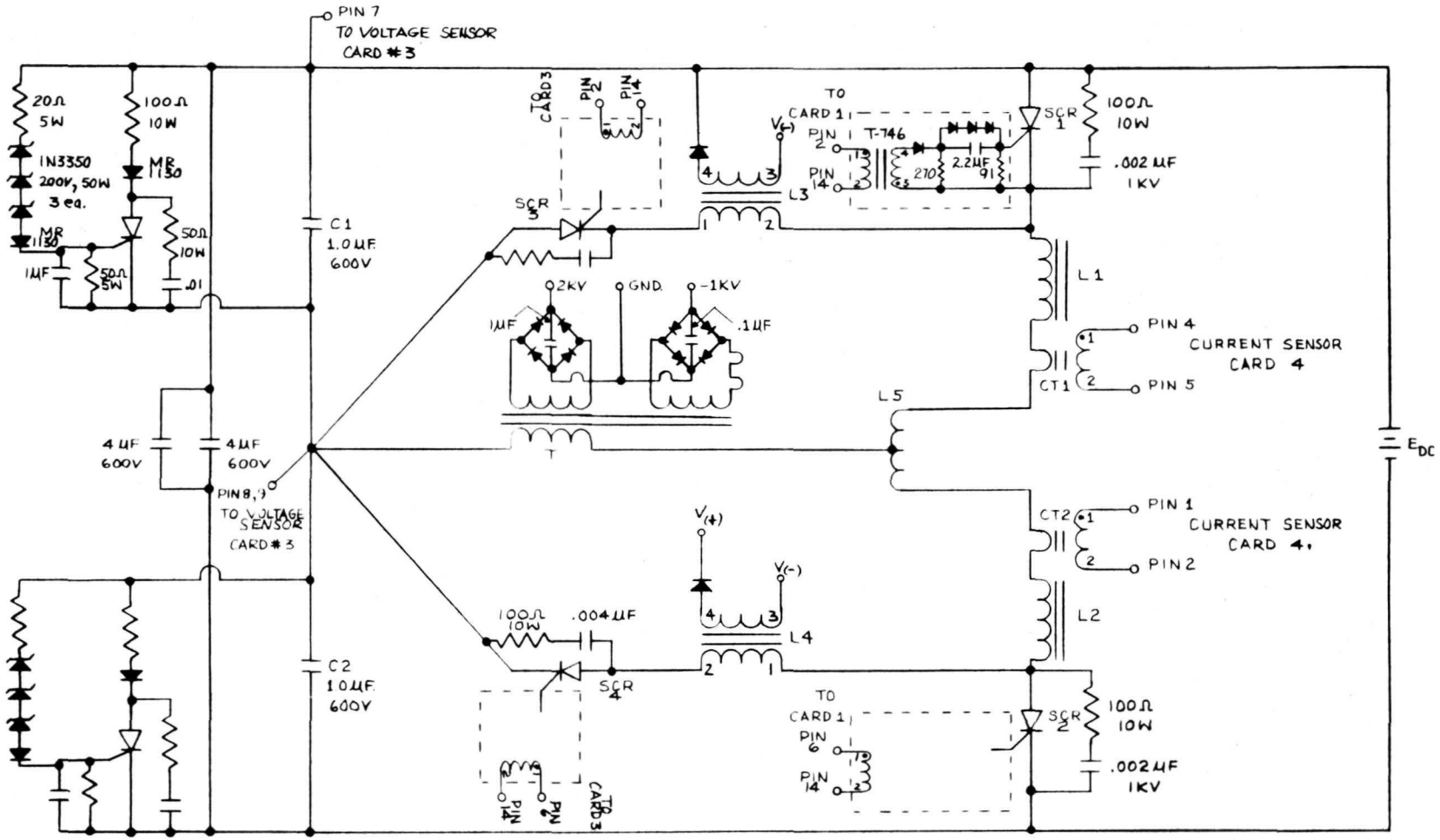
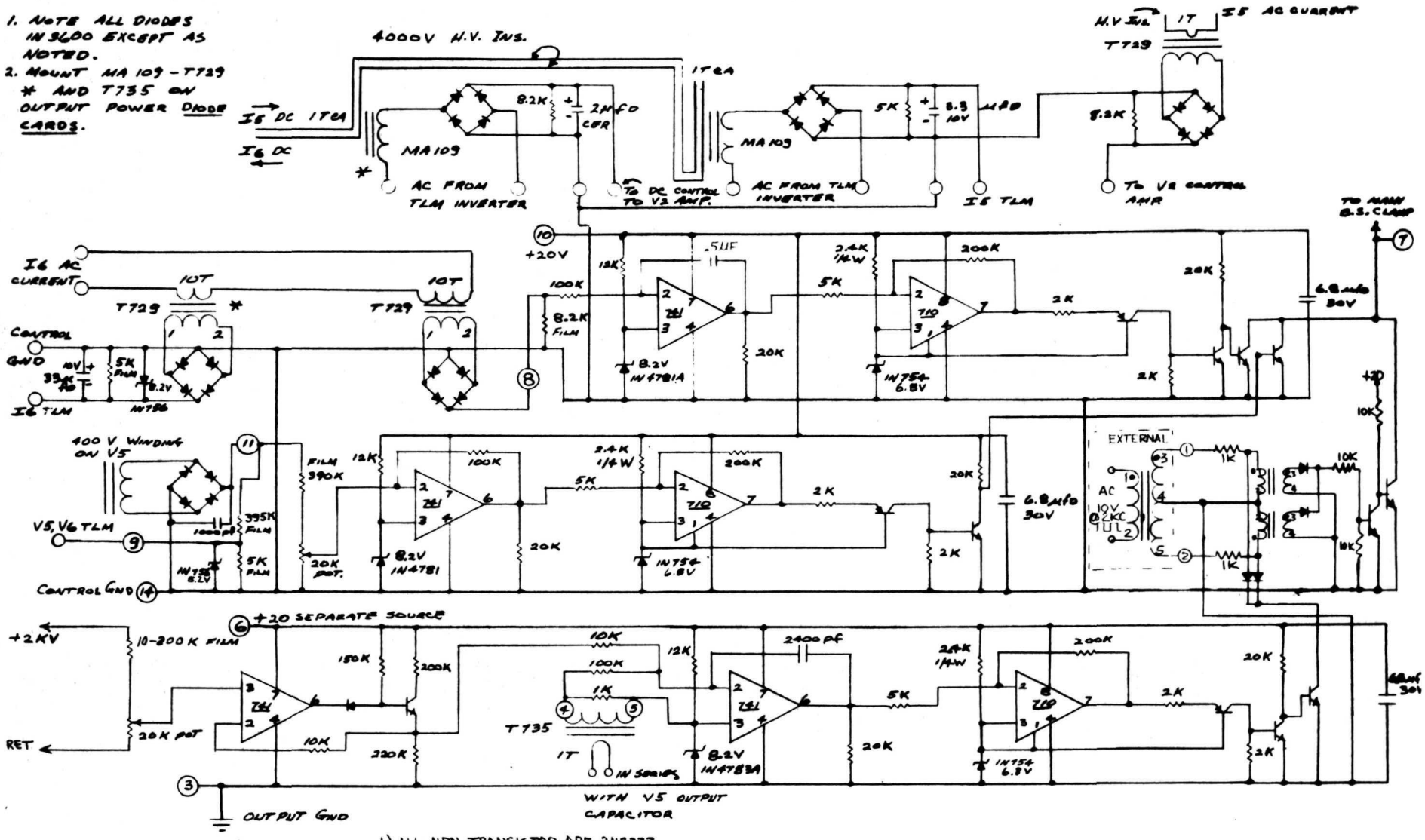


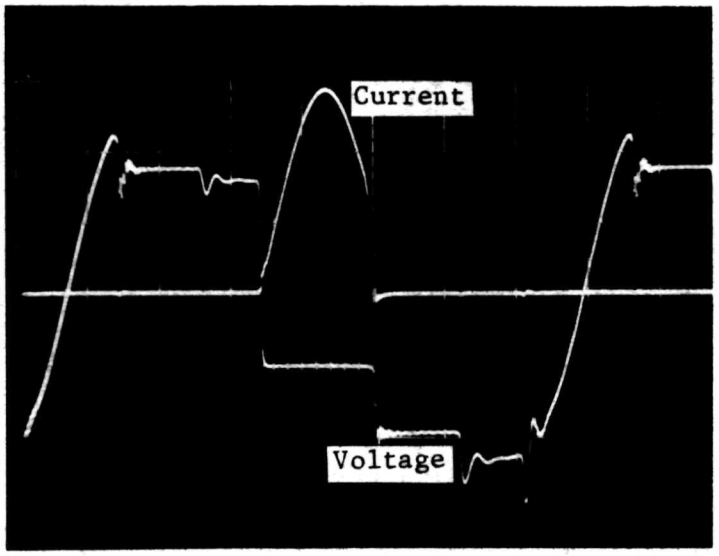
FIGURE 5-10 BEAM SERIES SCR INVERTER



1.) ALL NPN TRANSISTOR ARE 2N2222
2) ALL PNP TRANSISTOR ARE 2N2907A
3.)ALL DIODES ARE IN3600

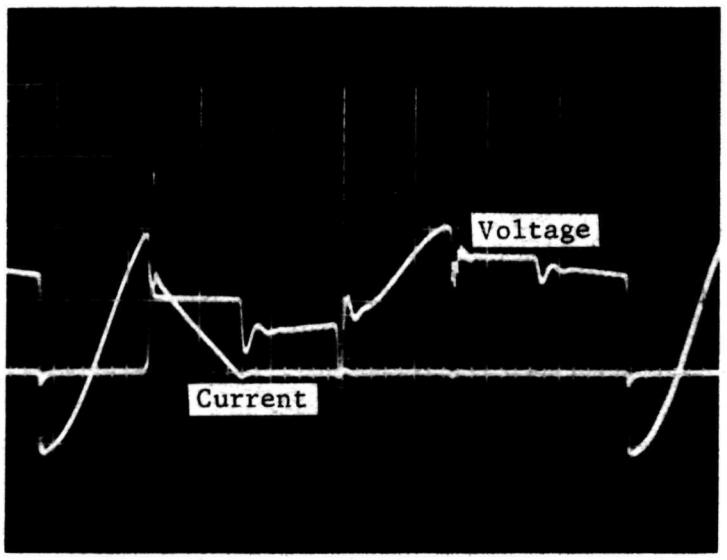
NOTES: UNLESS OTHERWISE SPECIFIED

FIGURE 5-11 V5 & V6 CONTROL AMPLIFIER



Main Line SCR
Voltage
Current

V = 200V/CM
I = 20A/CM
T = 20μs/CM



Auxiliary SCR
Voltage
Current

V = 200V/CM
I = 20A/CM
T = 20μs/CM

Beam Inverter

Figure 5-12 Photos of SCR voltage/current

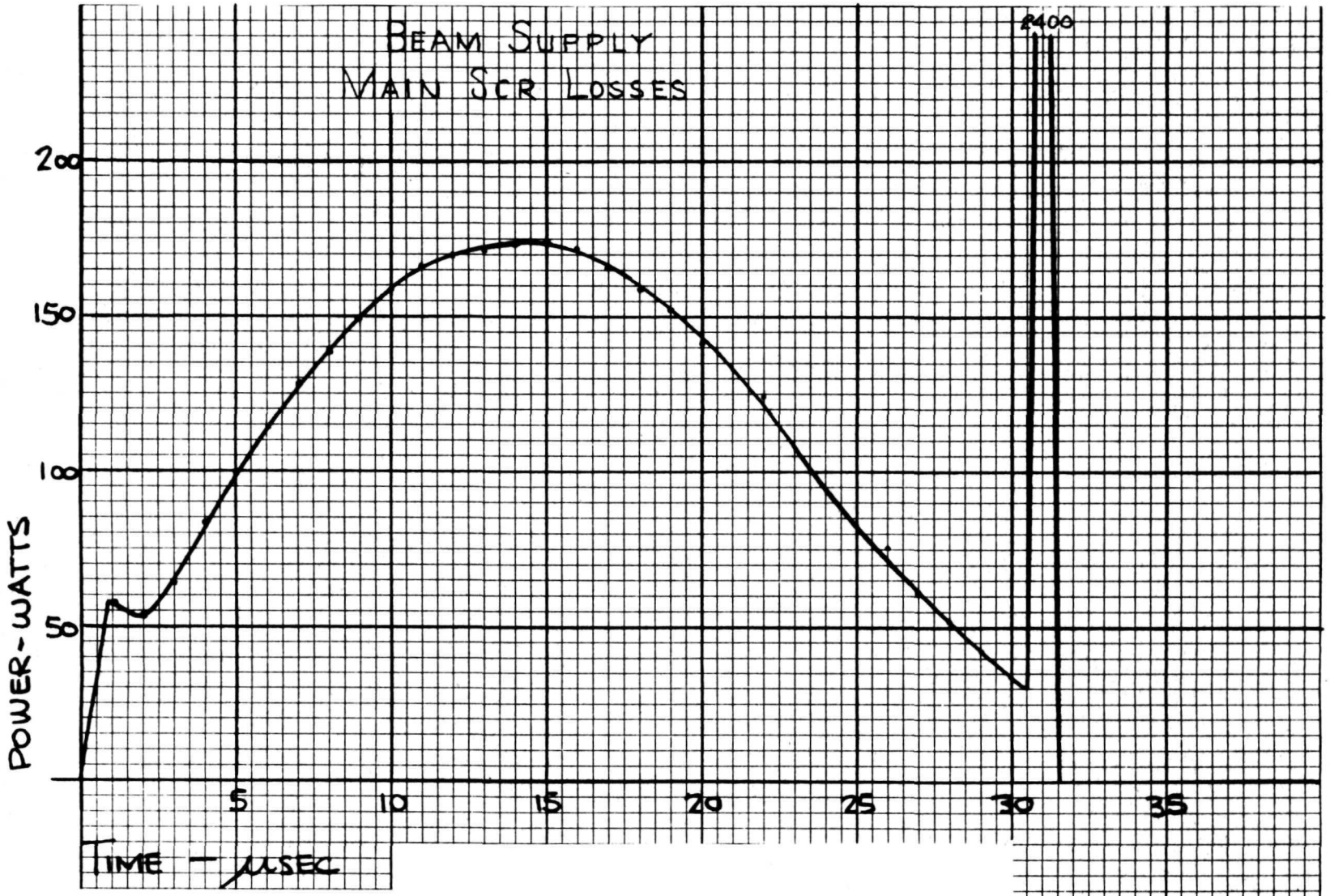


FIGURE 5-13A PLOT OF INSTANTANEOUS POWER VS TIME FOR MAIN LINE SCR

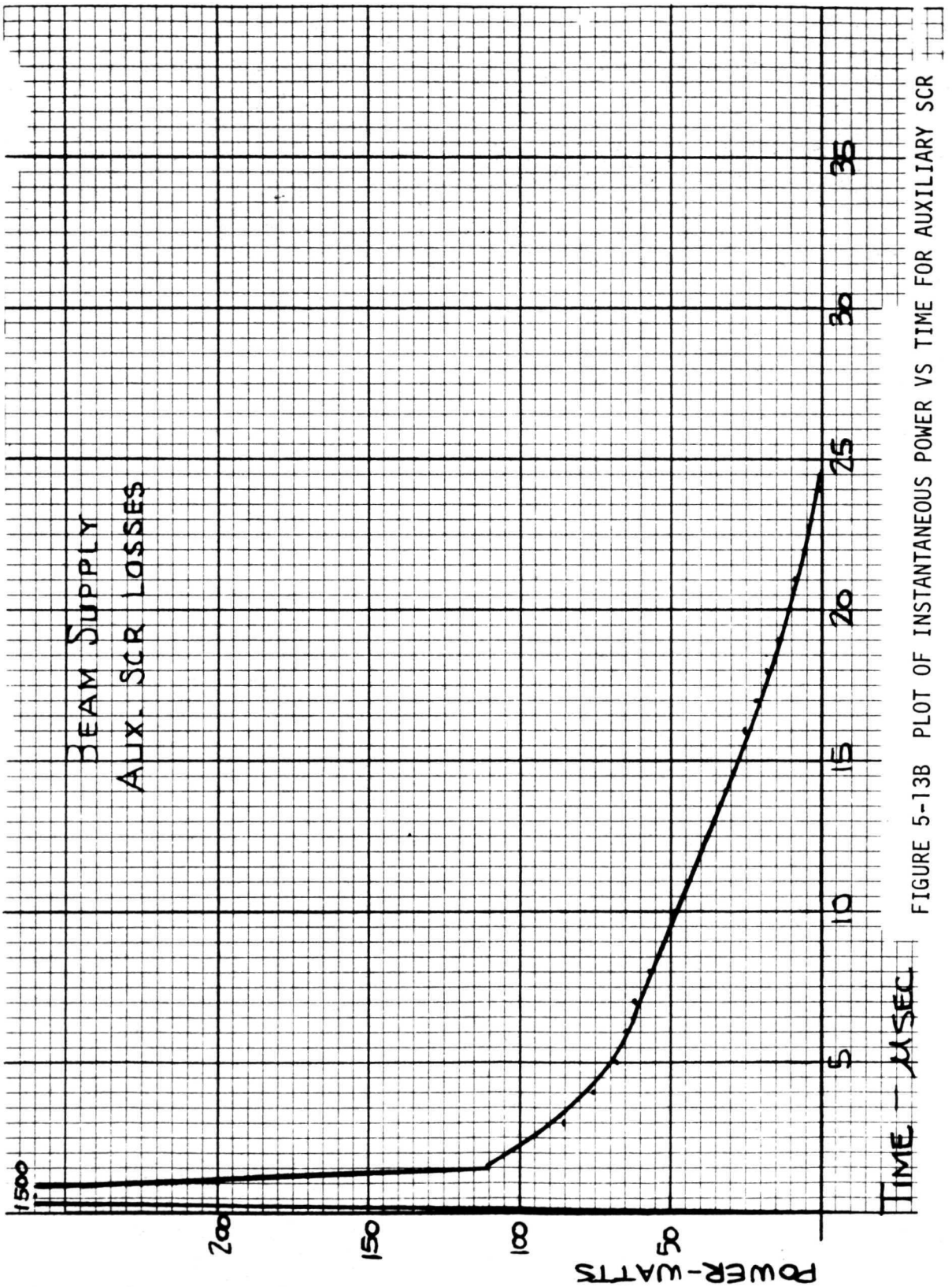


FIGURE 5-13B PLOT OF INSTANTANEOUS POWER VS TIME FOR AUXILIARY SCR

The output voltage variation from half load to full load was 2 volts.

Figure 5-14 is a plot of beam supply efficiency vs input voltage. Two curves are plotted. The new layout curve is a result of cleaning up the breadboard wiring which reduced the total resonant inductance. This reduction in inductance caused a higher peak current to exist thereby increasing the I2R losses and reducing the inverter efficiency. The rapid loss of efficiency with increase of voltage is caused by the higher loss that occurred when the auxiliary SCR is fired and the main line SCR is turned off. As the line voltage is increased the switching frequency is reduced to maintain output regulation thereby reducing the average switching losses and improving efficiency.

5.4 Arc Supply (V4)

Figure 5-15 illustrates the schematic of the SCR inverter power stage for the arc supply. The schematic of control logic is shown in Figure 5-3 through 5-7.

The arc supply control amplifier has been incorporated into the breadboard and is operating satisfactorily. The control amplifier schematic is shown in Figure 5-16.

The control amplifier has two feedback loops.

- V4 Voltage limiting
- I4 Current regulation

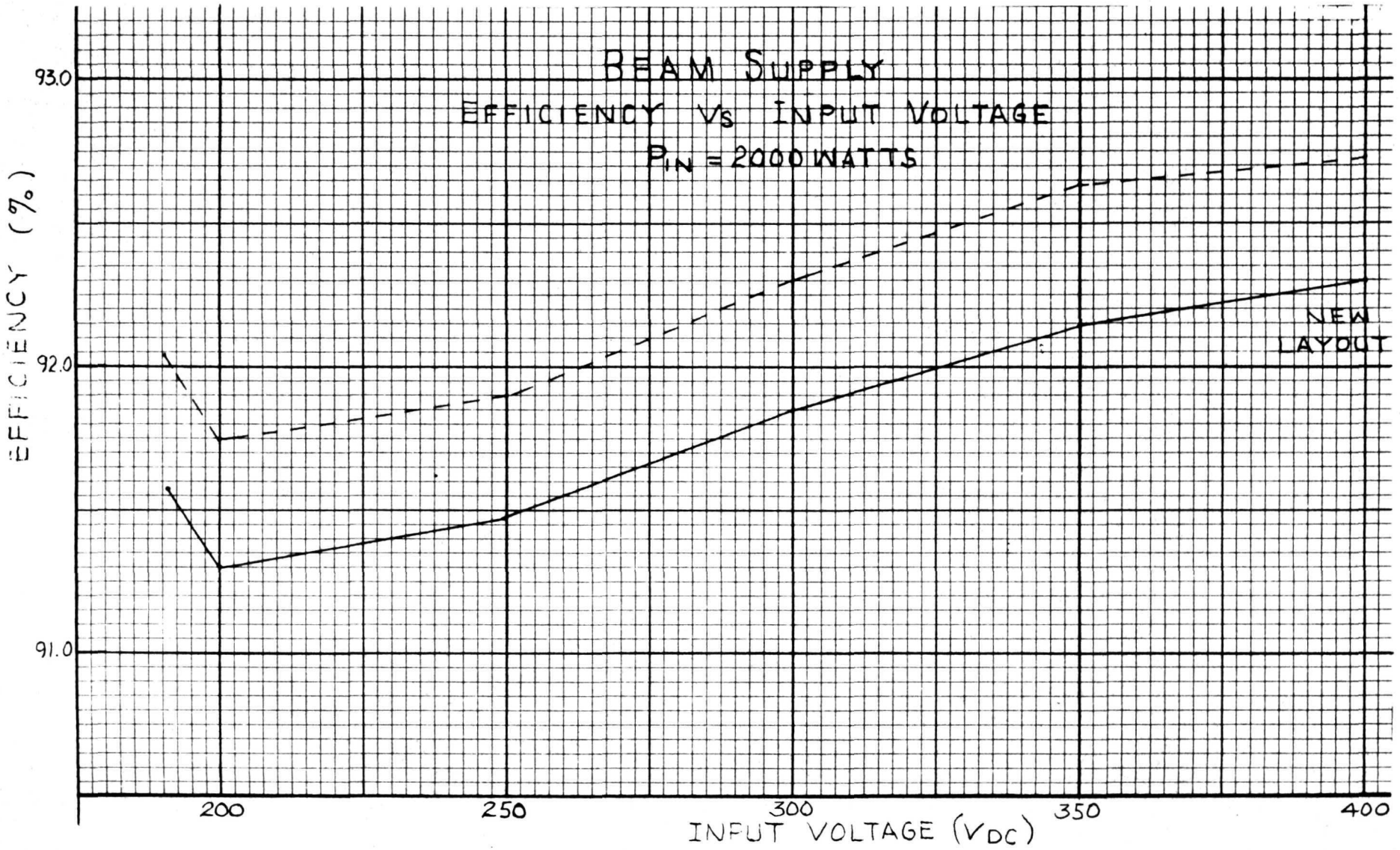


FIGURE 5-14 BEAM SUPPLY EFFICIENCY

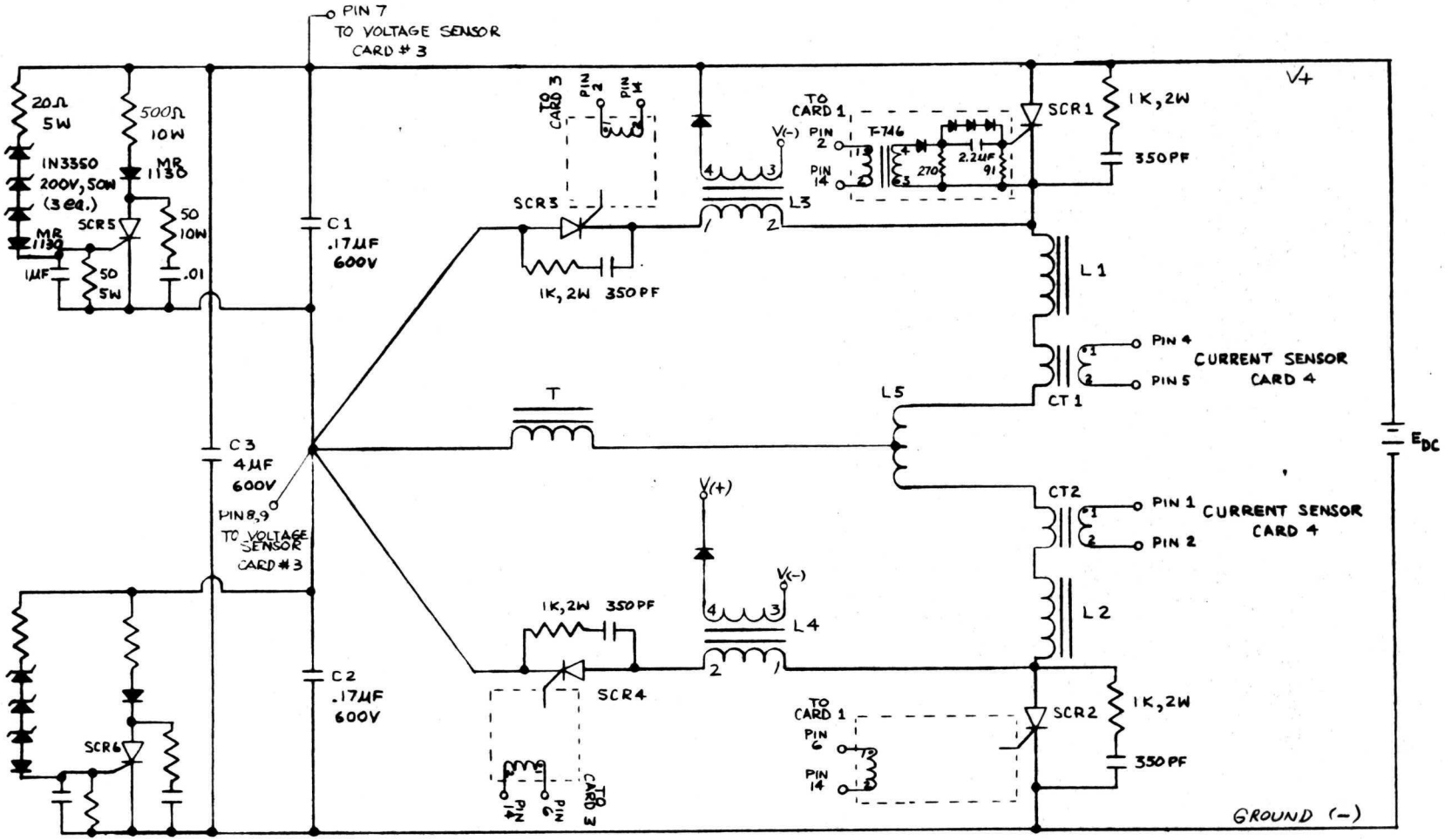


FIGURE 5-15 ARC SERIES SCR INVERTER

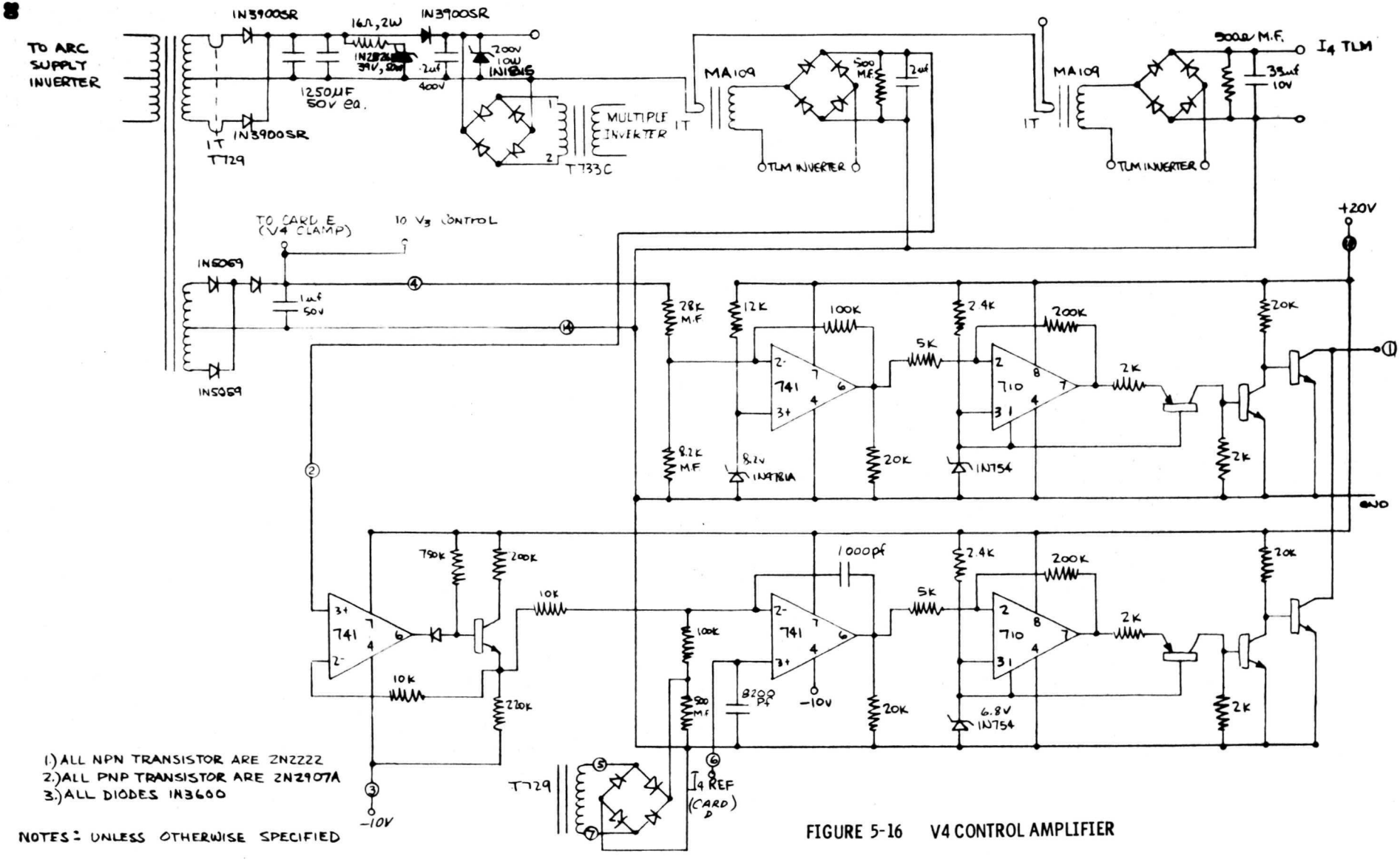
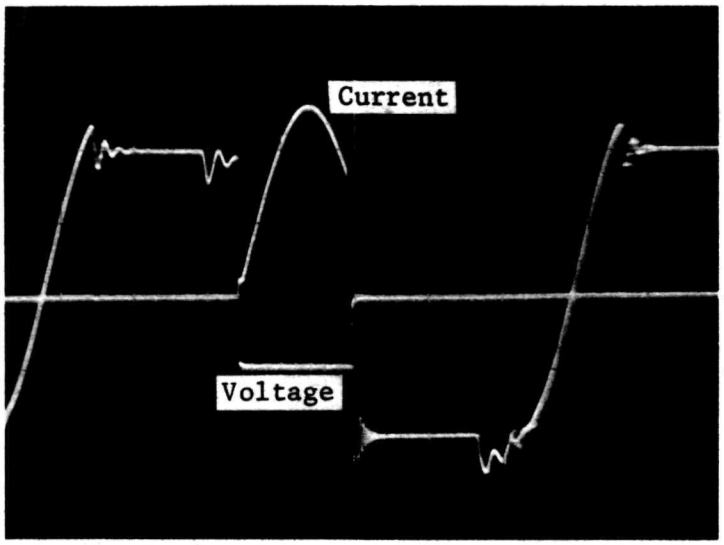


FIGURE 5-16 V4 CONTROL AMPLIFIER

V4 voltage limiting is provided by sensing the voltage on an isolated winding of the output transformer. I4 current regulation incorporates the ASDTIC two loop concept. Loop 1 senses the DC load current and loop 2 senses the AC output current. The two loops are combined and integrated and compared with a threshold level to actuate a threshold detector which activates the inverter power switch to control regulation.

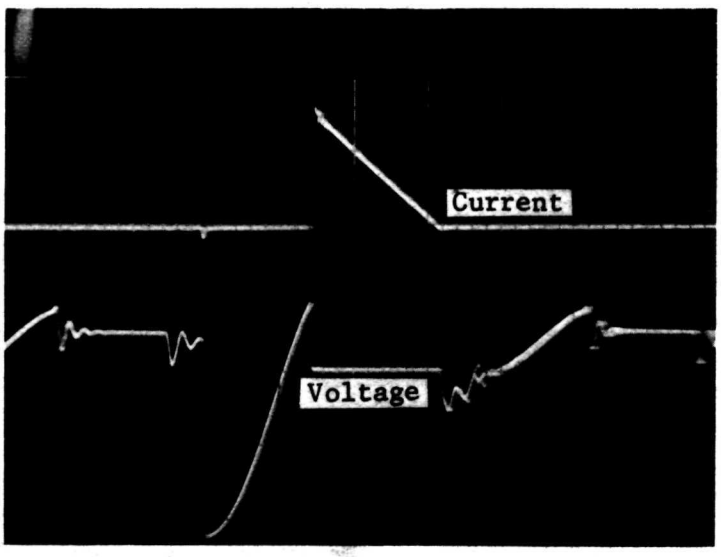
The arc supply circuit waveform photographs of the main line and auxiliary SCR voltage and current are presented in Figure 5-17.

A plot of efficiency vs supply voltage is shown in Figure 5-18. Figure 5-19 shows the output current regulation as a function of input line and temperature. The current regulation error is due to the variation in excitation circuit of the current transformer.



Main Line SCR
Voltage
Current

V = 200V/CM
I = 4A/CM
T = 20μs/CM



Auxiliary SCR
Voltage
Current

V = 200V/CM
I = 4A/CM
T = 20μs/CM

Figure 5-17 Photo of SCR Voltage/Current

Arc Inverter

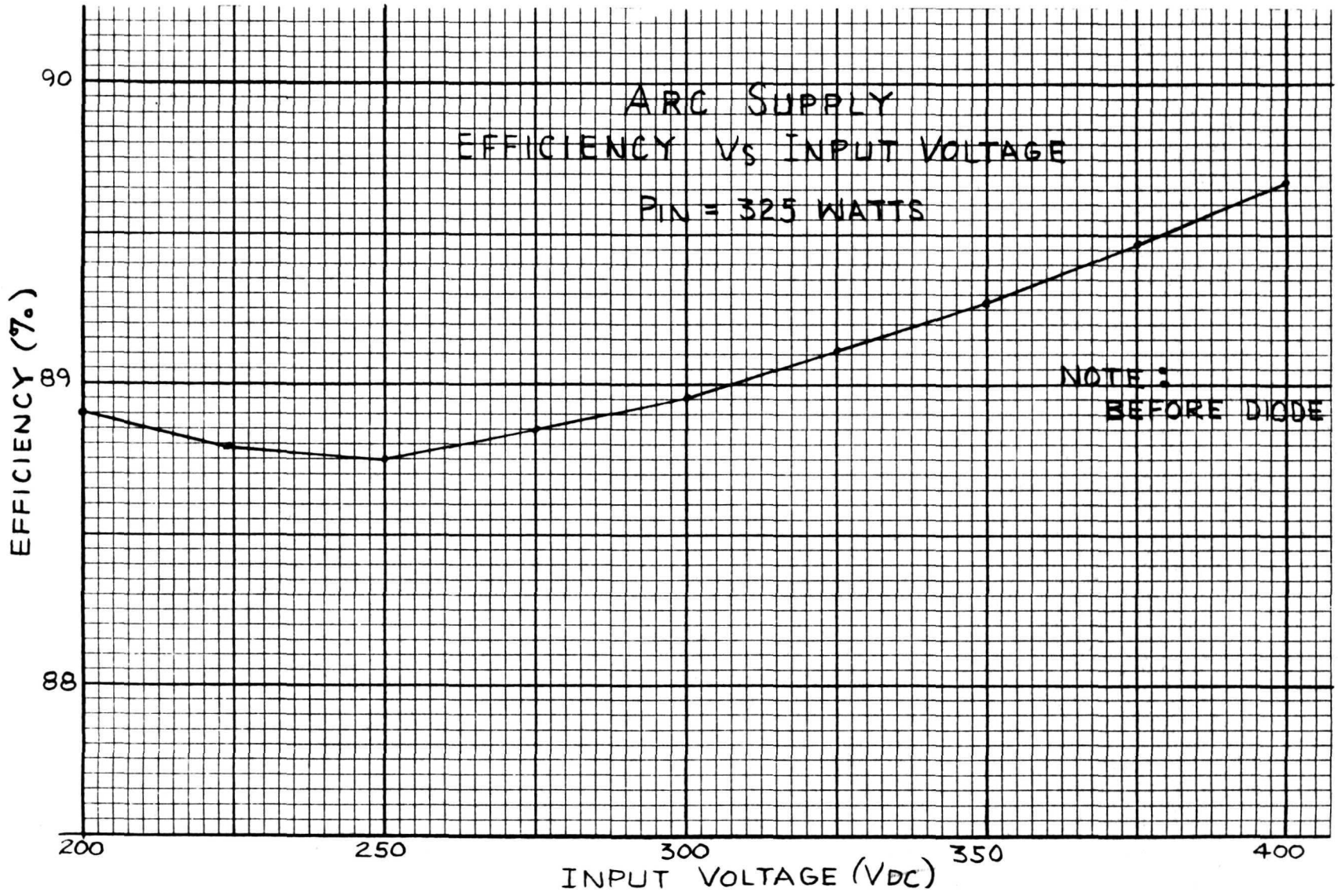


FIGURE 5-18 ARC SUPPLY EFFICIENCY

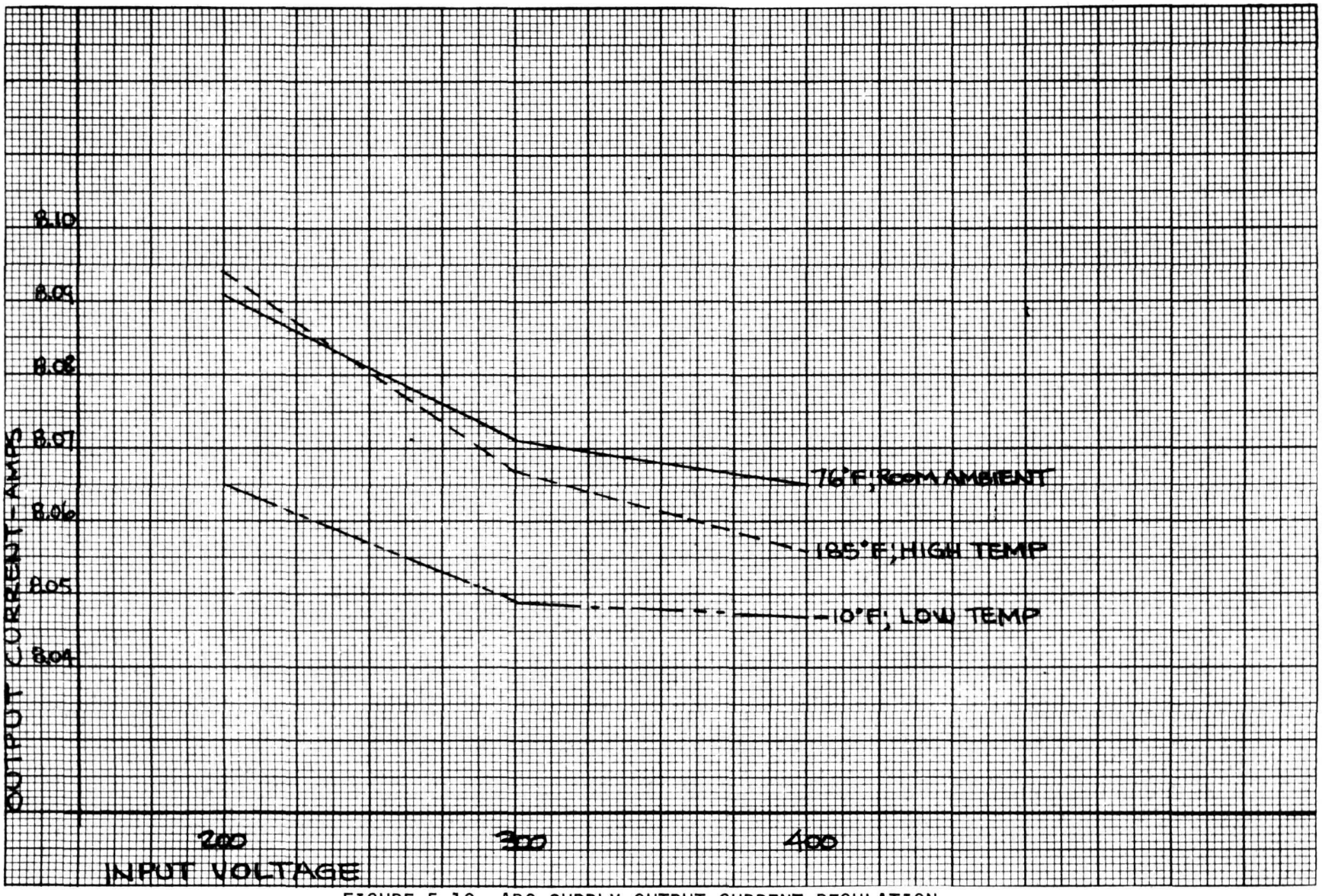


FIGURE 5-19 ARC SUPPLY OUTPUT CURRENT REGULATION

5.5 Multiple Output Inverter

The Multiple output inverter consists of the inverter power stage and regulators for each of the following supplies: V1, V2, V3, V7, V8, V9, V10, and Vaux. Also discharge supplies for V4, V8 and V10.

5.5.1 Inverter Power Stage

Inverter power stage schematic is shown in Figure 5-20. The output transformers of each supply are connected in series and located as shown. The SCR control logic schematics are shown in Figures 5-3 through 5-7. Figure 5-21 shows the current and voltage for the main line and auxiliary SCR.

5.5.2 V1 Supply (Magnet Supply)

Figure 5-22 shows the schematic of the V1 Supply. This supply has two regulating loops.

- V1 voltage limiting
- I1 current regulation

The voltage control loop limits the maximum voltage value. The current regulating loop utilizes the ASDTIC principle to regulate the current.

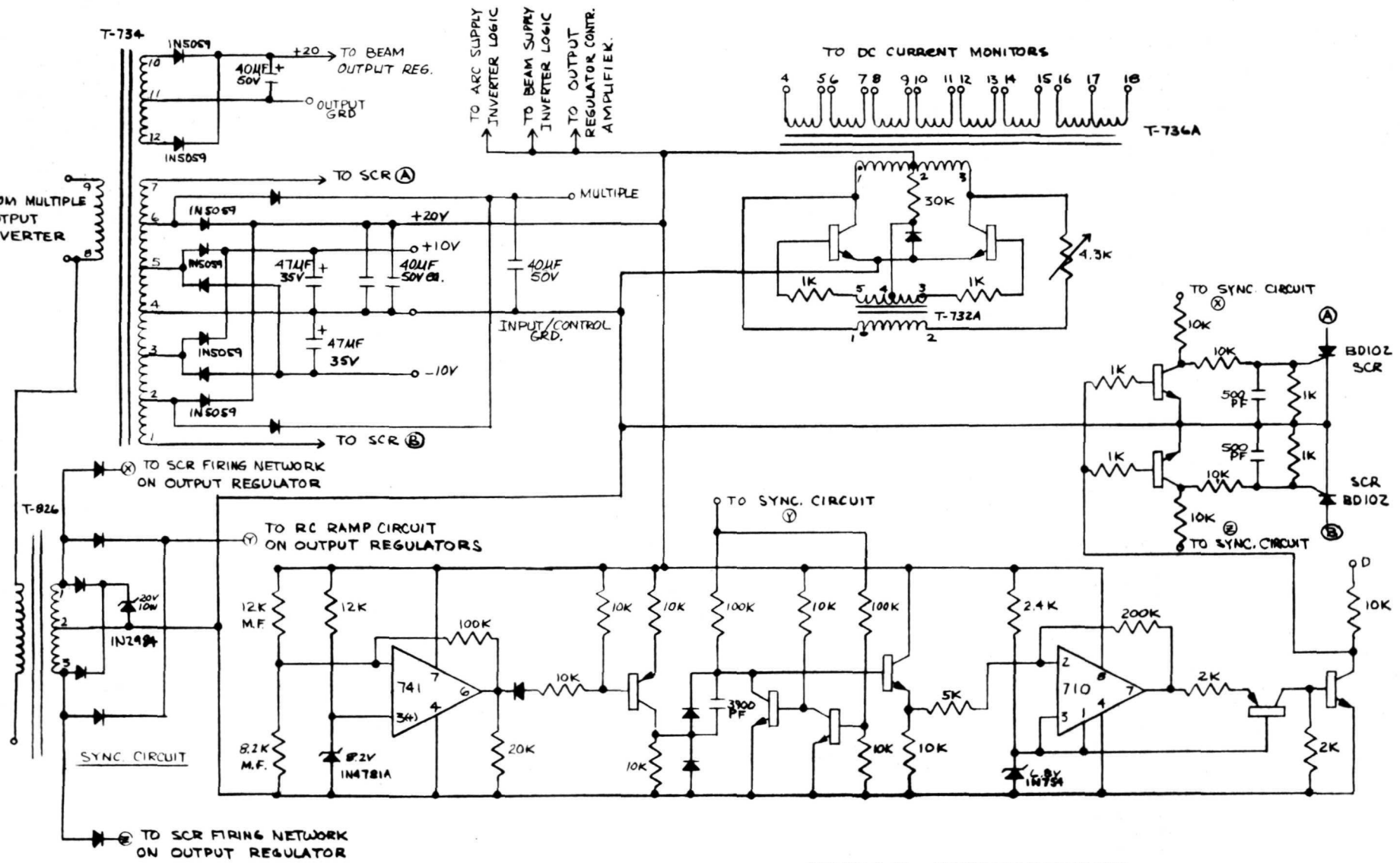
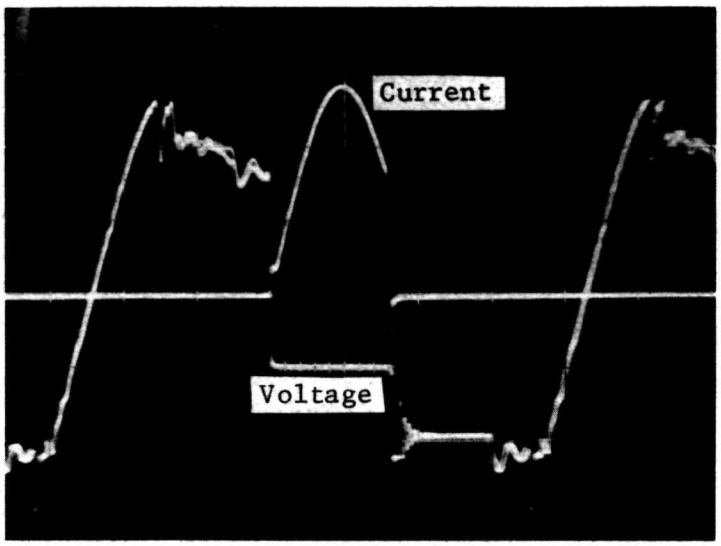
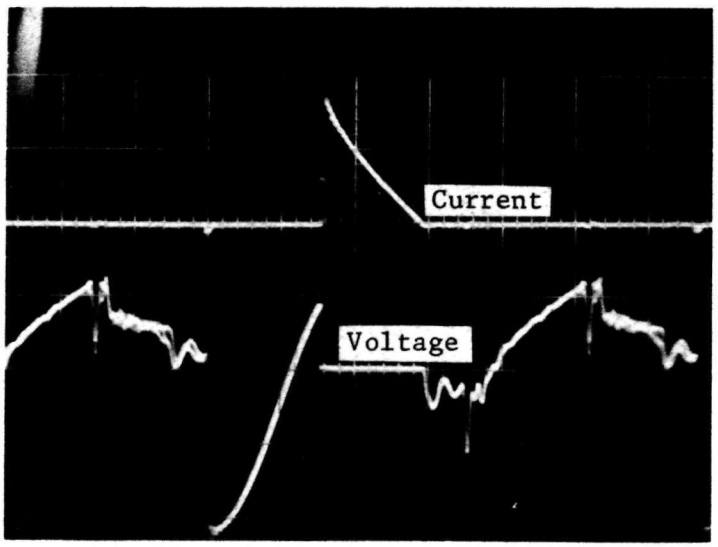


FIGURE 5-29 AUXILIARY OUTPUT AND TELEMETRY INVERTER



Main Line SCR
Voltage
Current

V = 200V/CM
I = 2A/CM
T = 20μs/CM



Auxiliary SCR
Voltage
Current

V = 200V/CM
I = 2A/CM
T = 20μs/CM

Multiple Inverter

Figure 5-21 Photos of SCR Voltage/Current

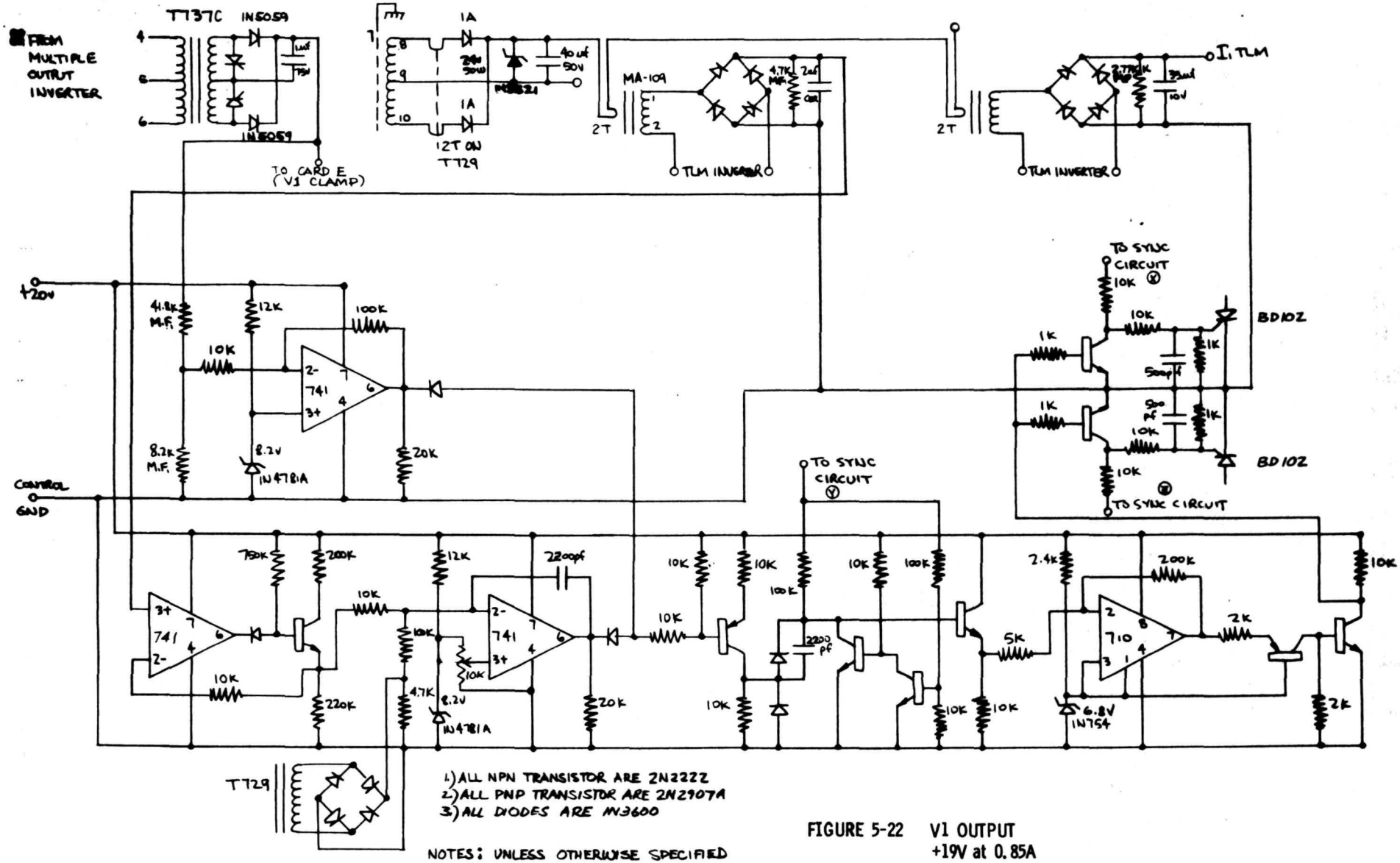


FIGURE 5-22 V1 OUTPUT
+19V at 0.85A

5.5.3 V2 Supply (Vaporizer Supply)

Figure 5-23 shows the schematic of the V2 supply. This supply has three regulating loops.

- V2 voltage limiting
- I2 current limiting
- I5 current control

The voltage control loop limits the maximum voltage value. The current control loop limits the maximum current value. The I5 current control loop regulated I5 current by varying the power of the V2 supply. The I5 current control loop incorporates the ASDTIC amplifier for control.

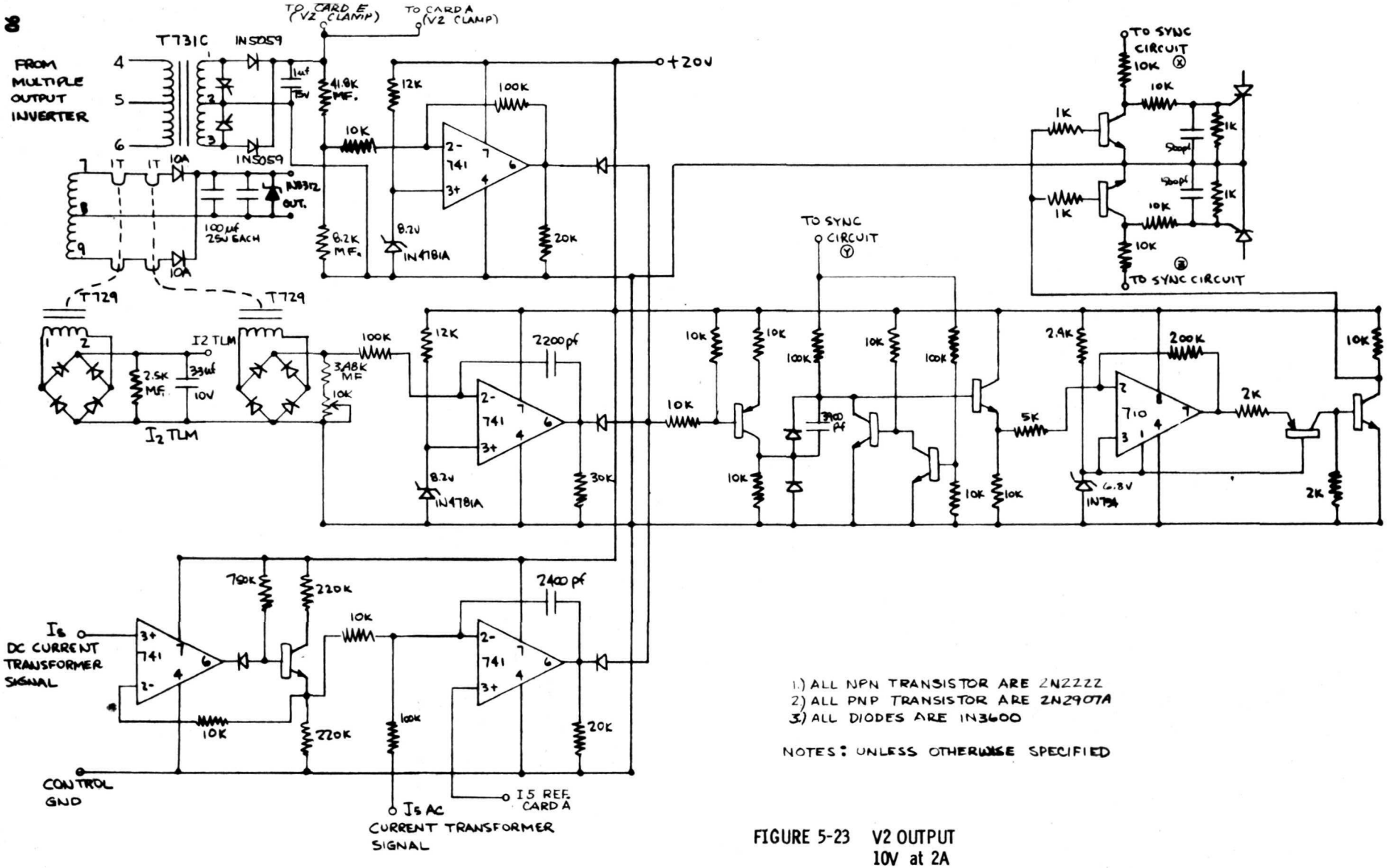
5.5.4 V3 Supply (Cathode Heater Supply)

Figure 5-24 shows the schematic of the V3 Supply. This supply has three regulating loops.

- V3 voltage limiting
- I3 current limiting
- V4 voltage regulator

The V3 voltage limiting and I3 current limiting loops control the maximum voltage and current output of the supply.

The V4 voltage regulator loop controls V4 voltage by varying V3 power.



1.) ALL NPN TRANSISTOR ARE 2N2222
2) ALL PNP TRANSISTOR ARE 2N2907A
3.) ALL DIODES ARE IN3600

NOTES: UNLESS OTHERWISE SPECIFIED

FIGURE 5-23 V2 OUTPUT
10V at 2A

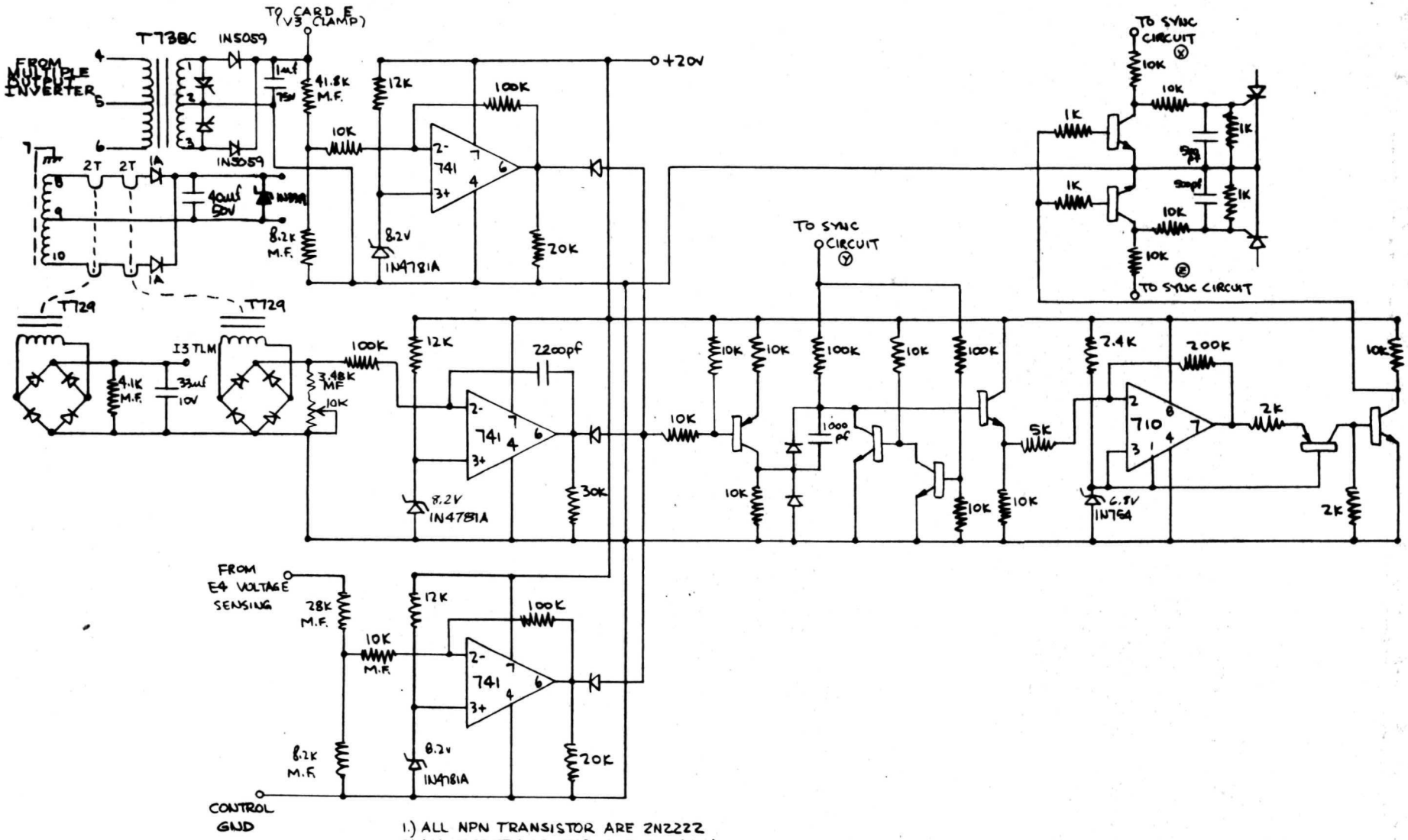


FIGURE 5-24 V3 Output
17V at 1A

5.5.5 V7 Supply (Neutralizer Heater Supply)

Figure 5-25shows the schematic of the V7 Supply. This supply has three regulating loops.

- V7 Voltage limiting
- I7 Current limiting
- V8 Voltage regulation

The V7 voltage limiting and I7 current limiting loops control the maximum voltage and current output of the supply. The V8 voltage regulation loop regulates V8 voltage by varying V7 power.

5.5.6 V8 Supply (Neutralizer Keeper Supply)

Figure 5-26 shows the schematic of the V8 supply. This supply has two regulating loops.

- V8 Voltage limiting
- I8 Current limiting

The V8 voltage limiting and I8 current limiting loops control the maximum voltage and current output of the supply.

5.5.7 V9 Supply (Cathode Tip Heater Supply)

Figure 5-27 shows the schematic of the V9 Supply. This supply has two regulating loops.

- V9 Voltage limiting
- I9 Current limiting

The V9 voltage limiting and I9 current limiting loops control the maximum voltage and current output of the supply.

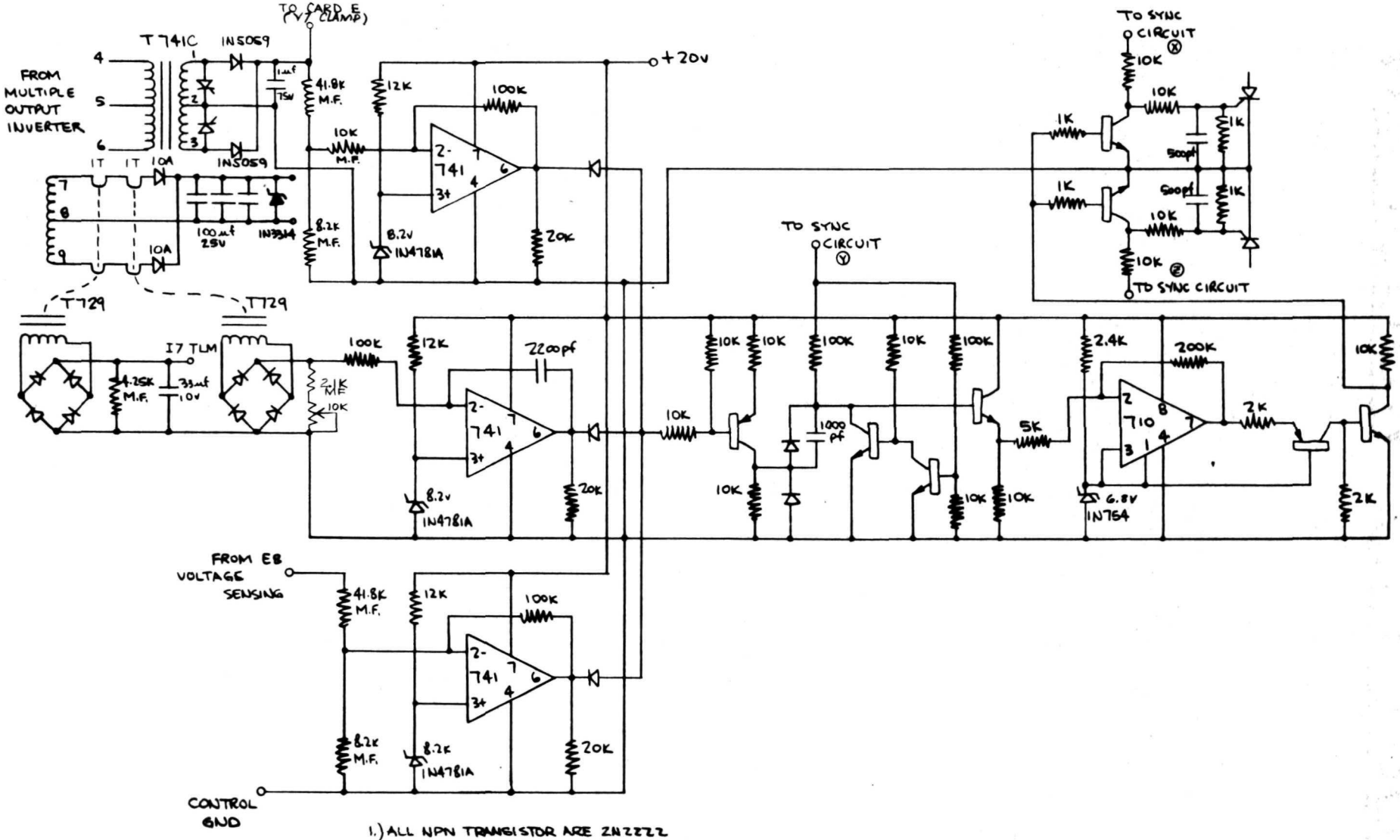
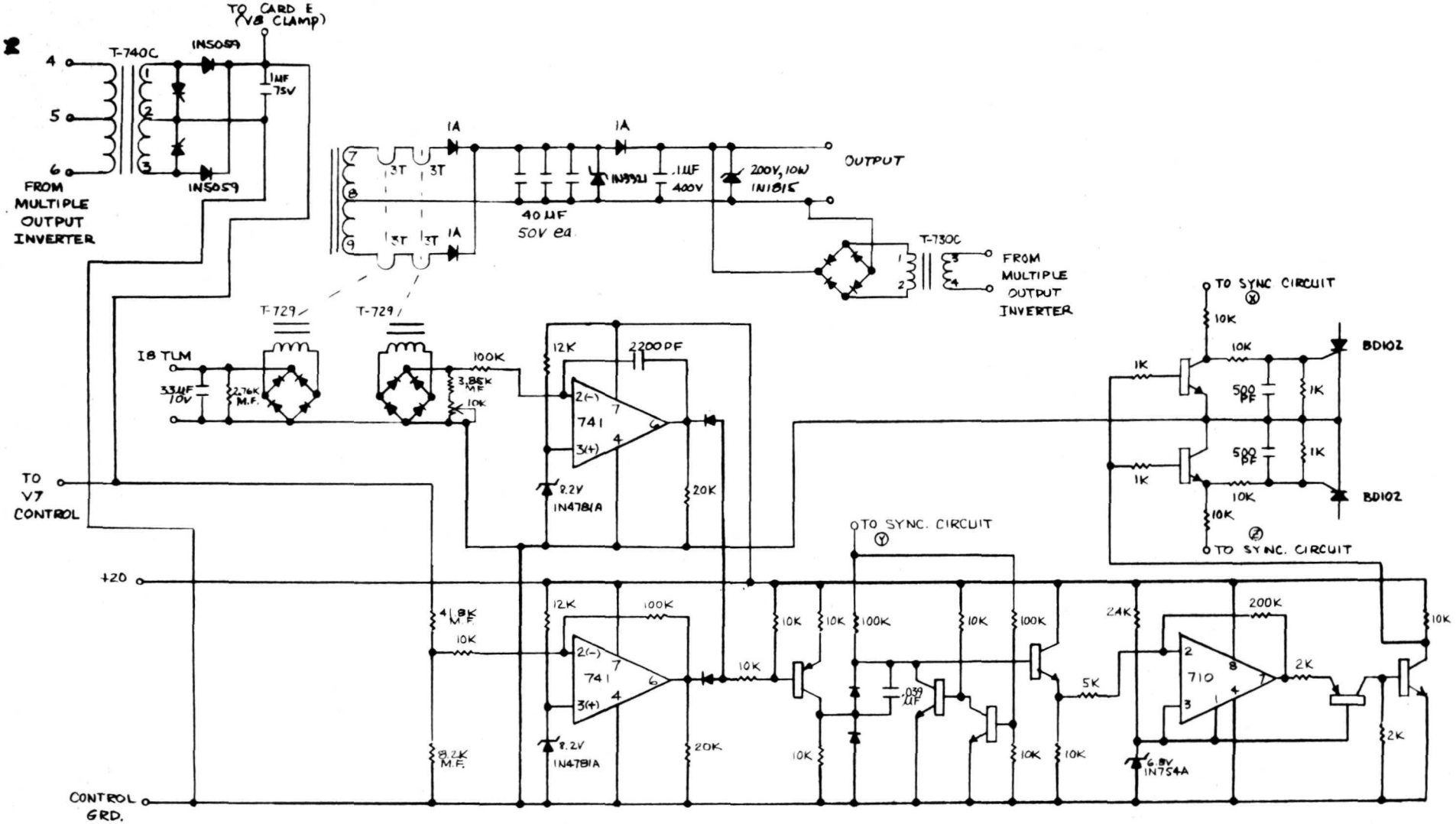


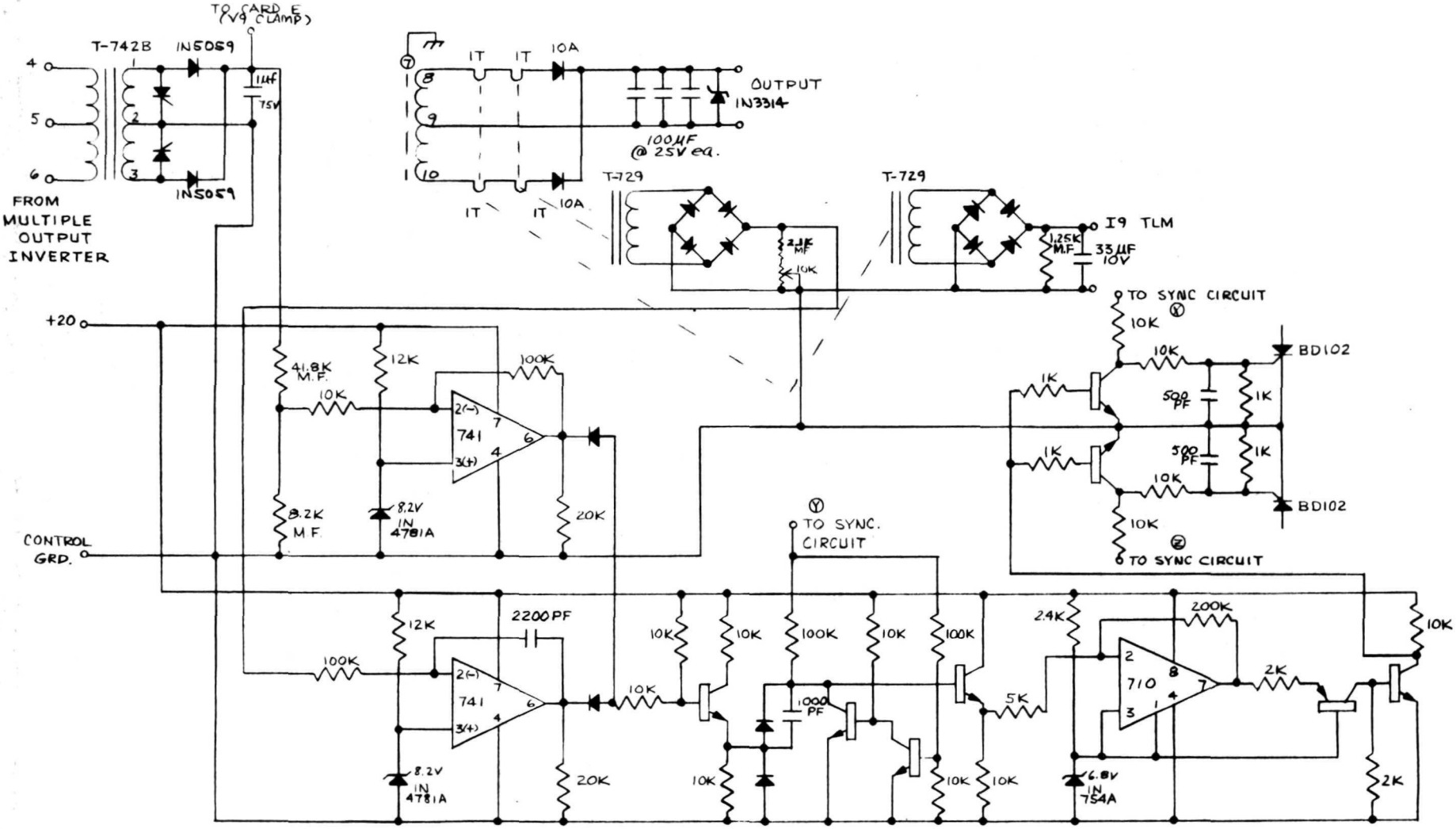
FIGURE 5-25 V7 OUTPUT
12V at 3.8A



1.) ALL NPN TRANSISTOR ARE 2N2222
2.) ALL PNP TRANSISTOR ARE 2N2907A
3.) ALL DIODES ARE IN3600

NOTES: UNLESS OTHERWISE SPECIFIED

FIGURE 5-26 V8 OUTPUT
20V at 0.6A



1.) ALL NPN TRANSISTOR ARE 2N2222
2.) ALL PNP TRANSISTOR ARE 2N2907A
3.) ALL DIODES ARE IN3600

NOTES: UNLESS OTHERWISE SPECIFIED

FIGURE 5-27 V9 OUTPUT 12V at 3A

5.5.8 V10 Supply (Cathode Keeper Supply)

Figure 5-28 shows the schematic of the V10 Supply. This supply has two regulating loops.

- V10 voltage limiting
- I10 current limiting

The V10 voltage limiting and I10 current limiting loops control the maximum voltage and current output of the supply.

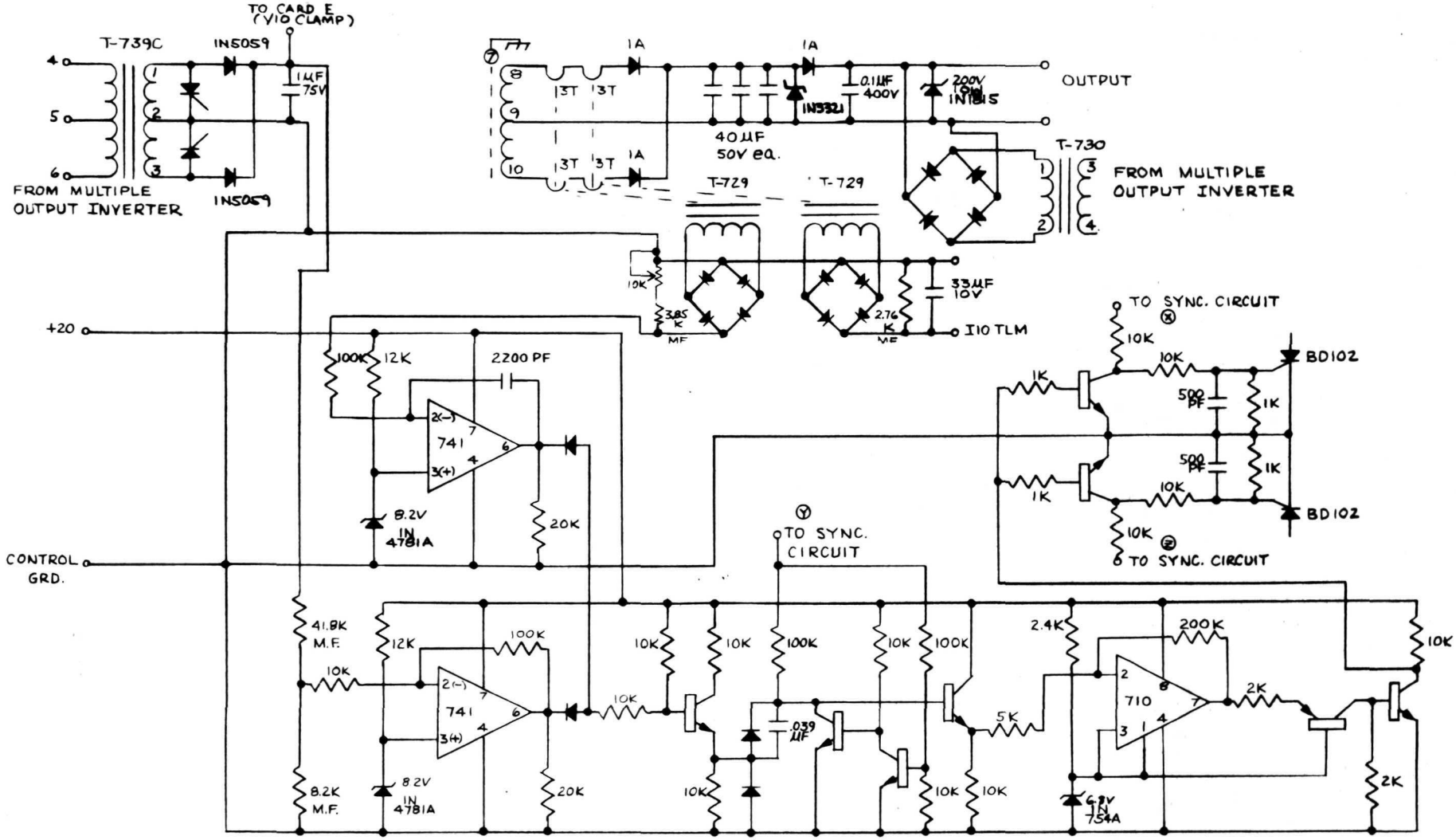
5.5.9 Discharge supplies for V4, V8, and V10

Discharge supplies for V4, V8, and V10 provide the high voltage at low currents necessary for initiating a discharge. It consists of a current transformer (T-730) in series with the primary of the power transformer, and a full wave bridge connected to the output.
See Figures 5-16, 5-26, and 5-28.

5.5.10 Vaux. Supply

Figure 5-29 shows the schematic of the auxiliary supply. This supply consists of:

- 20 VDC regulator to provide DC power to all the regulating and control circuits of the system.
- 2 KHz square wave oscillator to provide exciting voltage to the DC current monitors
- Sync circuit to provide synchronizing signals to the shorting SCR's in the output regulators.



1.) ALL NPN TRANSISTOR ARE 2N2222
2.) ALL PNP TRANSISTOR ARE 2N2907A
3.) ALL DIODES ARE IN3600

NOTES: UNLESS OTHERWISE SPECIFIED

FIGURE 5-28 V10 OUTPUT 20V at 0.6A

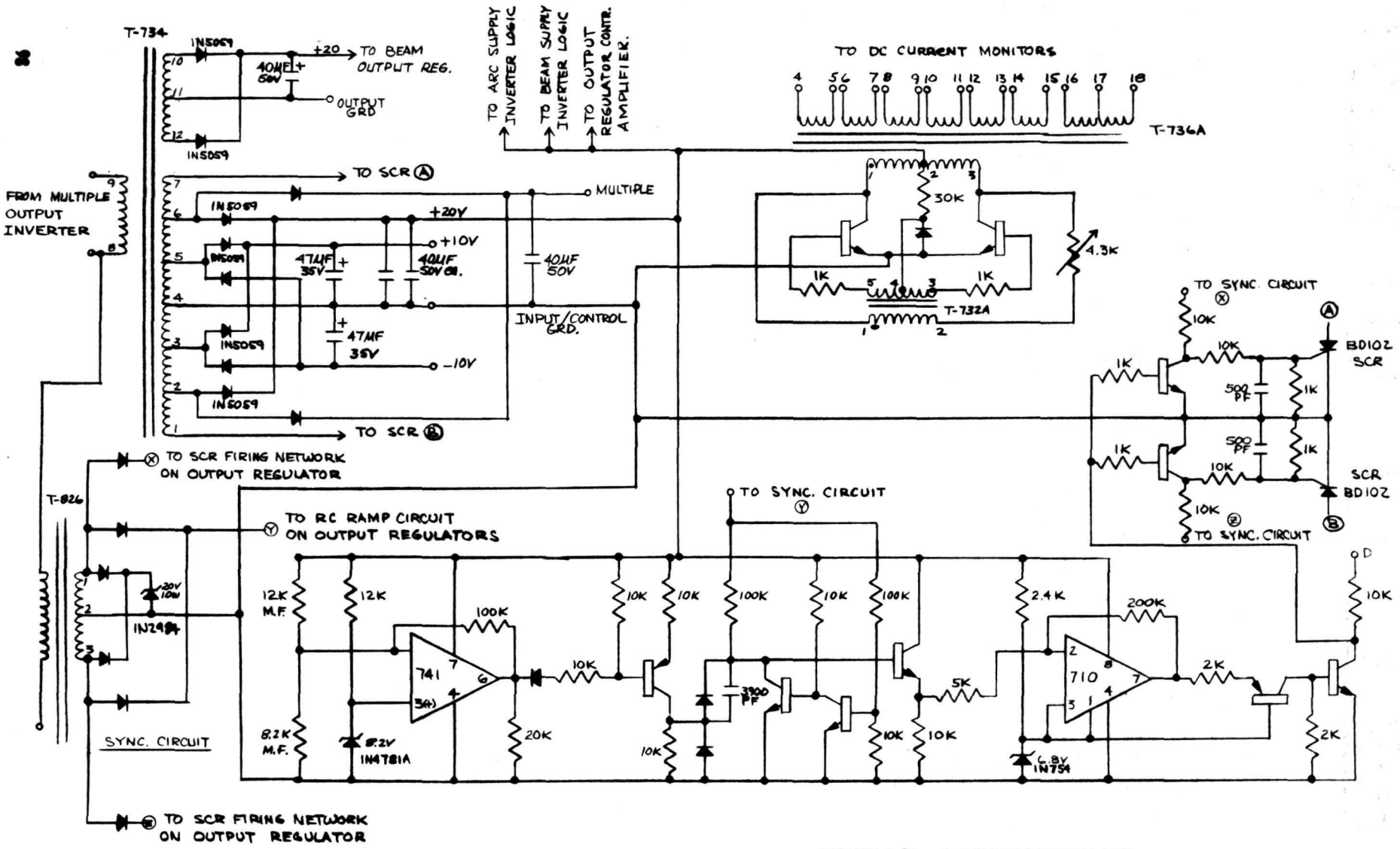


FIGURE 5-29 AUXILIARY OUTPUT AND TELEMETRY INVERTER

5.5.11 Multiple Output Regulator Stability Analysis

1. INTRODUCTION

Early in this work it was found that an inherent instability was caused by an increase of the ratio B/M, where B is the average load current, and M is the peak current of the power switch. It was found that, when the ratio reaches beyond a certain critical value (0.5 for the squarewave case), the regulated system becomes unstable. This drawback seriously limited the utilization of the regulating approach.

The problem was studied for possible remedies. One such means of correction has been analyzed and experimentally mechanized with favorable test results. Compared with the original system, the circuit modification has been kept minimum, while the stalbe operating range of the regulator is greatly extended without incurring major efficiency and weight penalties. The improvement is accomplished by adding another ramp function to the existing integrator ramp during the on-time of the power switch.

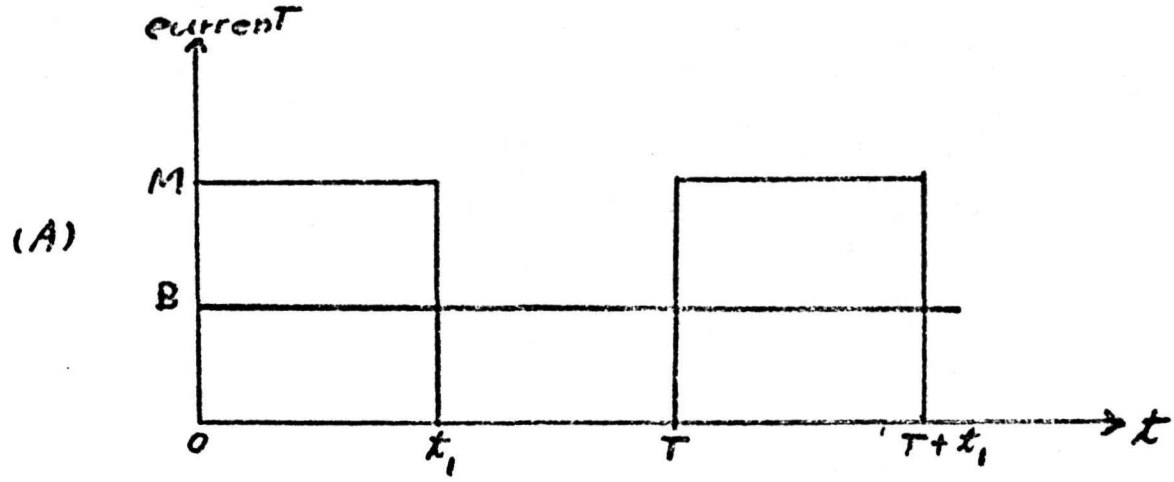
2. DESCRIPTION OF EARLY INSTABILITY PROBLEM

Using square-wave current for clarity, the current through the power switch and the corresponding integrator output of the original circuit are shown in Fig. 5-30A and B. In A, M and B are the peak and the average current of the power switch, respectively. The switch is turned on for a time interval t_1 within a period T. In B, e_T is the threshold voltage, and the slope of the integrator ramp during the time interval $T-t_1$ is BG/RC, where G is the current-to-voltage gain of the current sensor at the integrator input, and RC is the time constant of the integrator. During steady-state operation,

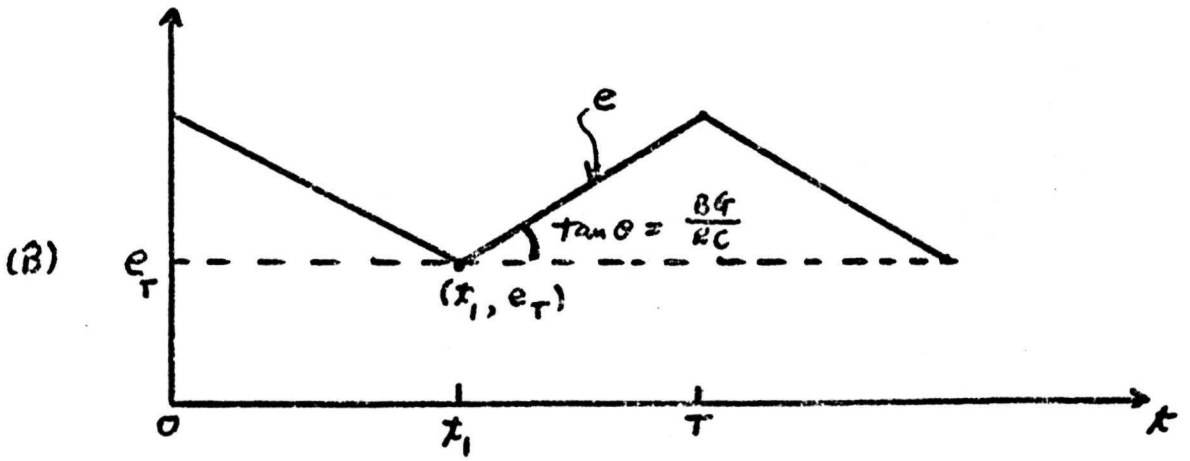
$$e-e_T = \frac{GB}{RC}(t-t_1) \qquad (1)$$

and

$$t_1 = \frac{Bt}{M} \qquad (2)$$



Current through the Power Switch.



Input Voltage to Threshold Detector

FIGURE 5-30 POWER SWITCH CURRENT AND INTEGRATOR OUTPUT VOLTAGE

From (1) and (2),

$$\Delta e = \frac{GT}{RCM} B(M-B) \tag{3}$$

The average voltage of the waveform shown in Fig. 5-30B is

$$\bar{e} = e_T + \frac{\Delta e}{2} = e_T + \frac{GTB(M-B)}{2RCM} \tag{4}$$

Differentiating (4) with respect to B gives

$$\frac{d\bar{e}}{dB} = \frac{GT}{2RCM} (M-2B) \tag{5}$$

Therefore,

$$\frac{d\bar{e}}{dB} > 0 \quad \text{as } M > B \tag{6}$$

$$< 0 \quad \text{as } M < B$$

Since there exists a phase inversion associated with the integrator, a further inversion such as caused by M < 2B would result in positive feedback, which leads inevitably to system instability. The instability would persist for all B's that are greater than M/2. The critical value of the ratio is therefore:

$$\frac{B}{M} = \frac{1}{2} \tag{7}$$

3. ANALYSIS OF THE MODIFIED SYSTEM

The revelant waveforms associated with the modified system are shown in Fig. 5-31. Fig. 5-31(A) illustrates the current through the power switch where $t_1 = BT/M$. The shaded area is effectively integrated without phase inversion in (B). The slope of the integrated waveform is G(M-B)/RC. The new circuit modification is expressed in (C) as a ramp with a slope K_r. The composite waveform shown in (D) is the input voltage to the threshold detector.

The straight line passing the point (t_1, e_T) with a slope $K_r + (G/RC)(M-B)$ is:

$$e-e_T = [K_r + \frac{G(M-B)}{RC}] (t-t_1) \tag{8}$$

This straight line intersects the axis t = 0 at

$$e_o = e_t - [K_r + \frac{G(M-B)}{RC}] \frac{BT}{M} \tag{9}$$

The waveform of Fig. 5-31(d) contains three areas, I, II and III. In terms of B and other circuit parameters, there areas can be expressed as:

$$\text{Area I} = e_oT = e_TT - [K_r + \frac{G(M-B)}{RC}] \frac{BT^2}{M} \tag{10}$$

$$\text{Area II} = \frac{1}{2} [K_r + \frac{G(M-B)}{RC}] t_1^2 = \frac{1}{2} [K_r \frac{G(M-B)}{RC}] (\frac{BT}{M})^2 \tag{11}$$

$$\text{Area III} = \frac{1}{2} \frac{G(M-B)}{RC} t_1(T-t_1) = \frac{1}{2} \frac{G(M-B)}{RC} \frac{BT}{M} \cdot \frac{M-B}{M} T \tag{12}$$

The average value of the sum of the three areas is:

$$\bar{e} = e_T - \frac{T}{2M^2} [K_r + \frac{G(M-B)}{RC}] B(2M-B) + \frac{TGB(M-B)^2}{2RCM^2} \tag{13}$$

Differentiating with respect to B gives

$$\frac{d\bar{e}}{dB} = \frac{T}{2M^2} [-2MK_r - \frac{GM^2}{RC} + \frac{2GMB}{2RC} + 2BK_r] \tag{14}$$

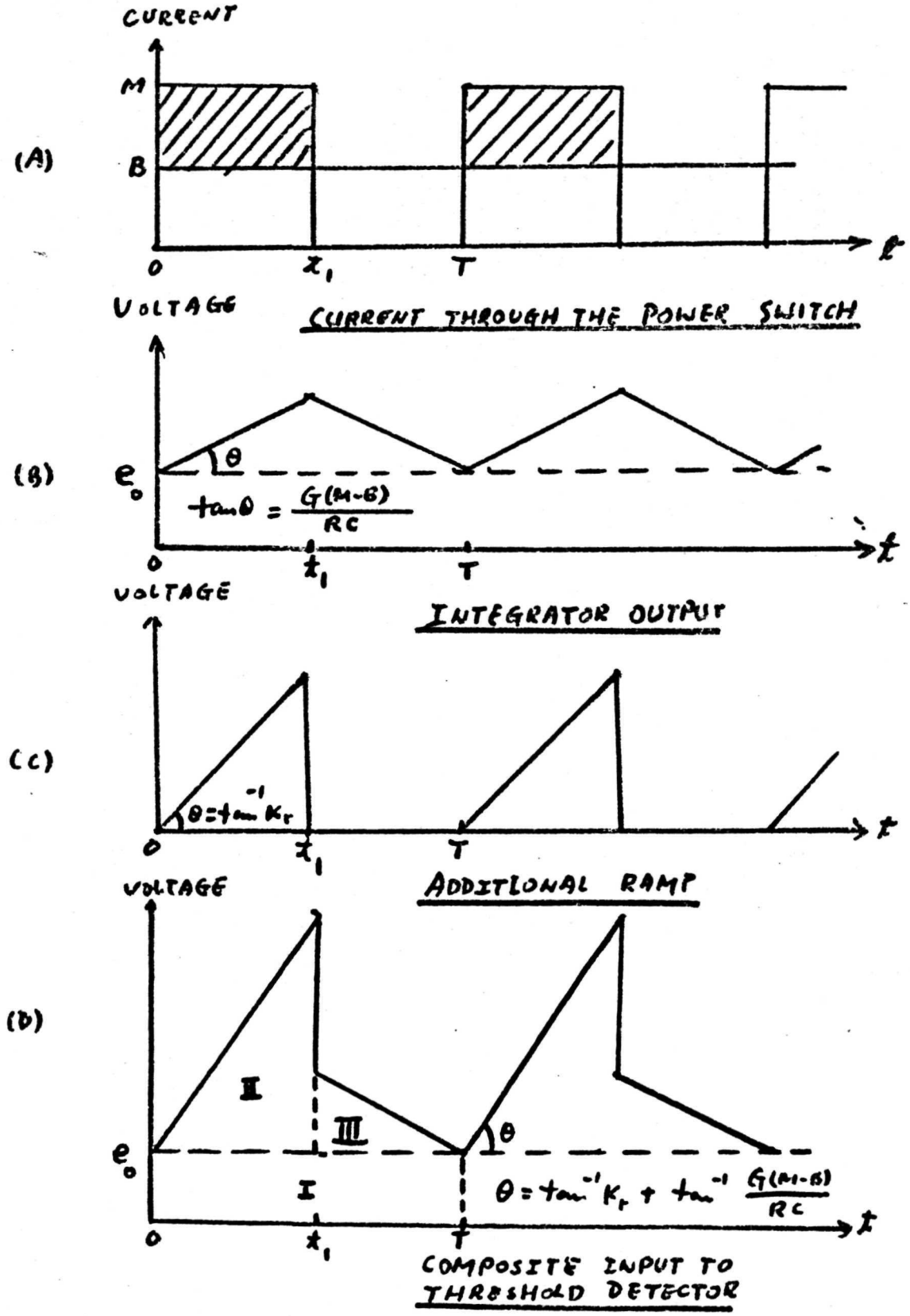


FIGURE 5-31 RELEVANT WAVEFORMS OF THE MODIFIED SYSTEM

Equation (14) vanishes when

$$\frac{B}{M} = \frac{2K_r + \frac{MG}{RC}}{sK_r + \frac{2MG}{RC}} \qquad (15)$$

This is the B/M ratio beyond which the system becomes unstable. Notice that when $K_r = 0$, i.e., no additional ramp, equation (15) reduces properly to eq. (7). As K_r increases, the critical B/M gradually increases from 1/2 and approaches unity as its upper limit. The function of the new ramp is therefore to extend the critical B/M ratio to higher value of B for a given M. It is with this mathematical background that the new circuit modification is successfully implemented.

4. ANALYSIS OF THE MODIFIED SYSTEM FOR THE SERIES INVERTER WITH QUASI-SINUSOIDAL CURRENT

While the function of the additional ramp on a squarewave regulator has been clearly demonstrated in the previous section, it remains to be analyzed the corresponding improvement when the ramp is applied to the more realistic current waveform in the series inverter where a quasi-sinusoidal pulse is followed by an essentially linear decay. Such a current waveform is illustrated in Fig. 5-32 (A) with a period T. The sinusoid starts at t=0, reaches a peak amplitude of M, and lasts until $t=t_3$, after which the current decays linearly to zero at $T-T_d$. A time interval T_d is provided to allow the complete turn-off of the SCR. Notice that, if the sinusoid were allowed to complete, its half period would be at t_2, where $0 < t3 < t2 < T-T_d < T$. Fig. 5-32(B) shows the part of the pulse from t=0 to $t=t_1$ that passes through the power switch to the load. The average value of this pulse over a period T is B. The shaded area shown in Fig. 3(B) is integrated, giving an output resembling that of Fig. 5-32(C). Together with the additional ramp shown in Fig. 5-32(D), the composite input voltage to the threshold detector is given in Fig. 5-32(E).

Let $m = \pi/t_2$ in Fig. 5-32(B), then,

$$B = \frac{1}{T}\left[\int_0^{t_3} M \sin mt\,dt + \left(M \sin mt_3 + \frac{T-t_1-T_d}{T-t_3-T_d} M \sin mt_3\right)\frac{(t_1-t_3)}{2}\right] \qquad (16)$$

Eauation (16) can be simplified to

$$B = \frac{M}{T}\left[\frac{1-\cos mt_3}{m} + \frac{(T-t_d)\sin mt_3}{-t_3-t_d}(t_1-t_3)\frac{\sin mt_3}{a(T-t_3-T_d}(t_1^2 - t_3^2)\right] \quad (17)$$

Solving (17) for t_1 and choosing the nontrivial solution gives

$$t_1 = I - \sqrt{Y + JB} \quad (18)$$

where

$$\begin{aligned} I &= T-T_d \\ Y &= L^2 + \frac{2K}{P} \\ J &= -\frac{2Y}{P} \\ L &= T - t_3 - T_d \\ P &= \frac{M \sin mt_3}{T-t_3-T_d} \\ K &= (M/m)(1 - \cos mt_3) \end{aligned} \quad (19)$$

Equation (18) relating t_1 to B can now be used to evaluate Δe_1 of Fig. 5-32(C),

$$\Delta e_1 = \frac{G}{RC}\left\{\int_0^{t_3}(M \sin mt - B)dt + \int_{t_3}^{t_1}\left[\frac{(M \sin mt_3)(T-T_d-t)}{T-t_3-T_d} - B\right]\right\} dt \quad (20)$$

where G is the current-to-voltage gain of the current sensor at the integrator input, and RC is the time constant of the integrator. Following simplification, equation (20) becomes

$$\Delta e_1 = \frac{G}{RC}\left[K - Bt_3 + (PI-B)(L - \sqrt{Y+JB}) - \frac{P}{2}(L - \sqrt{Y+JB})(A - \sqrt{Y+JB})\right] \quad (21)$$

where

$$A = T + t_3 - T_d \tag{22}$$

Since the sum of $e_o + \Delta e_1$ of Fig. 3(C) and Δe_2 of Fig. 5-32(D) must be equal to e_T at t_1, one has

$$e_o = e_T - \frac{G}{RC}[k-Bt_3+(P-B)(L-\sqrt{Y+JB}) - \frac{P}{2}(L-\sqrt{Y+JB})(A-\sqrt{Y+JB})] \tag{23}$$

$$- K_r(T-T_d - \sqrt{Y+JB}$$

Here, K_r is the slope of the ramp function in Fig. 5-32(D). Simplifying (23) yields

$$e_o = e_T-K_r(I-\sqrt{Y+JB})- \frac{G}{RC}[k-Bt_3+(Pt-B)(L-\sqrt{Y+JB})- \frac{P}{2}(AL-2t\sqrt{Y+JB+Y+JB})] \tag{24}$$

The average input to the threshold detector is thus

$$\bar{e} = \frac{1}{T} [e_oT + \frac{1}{2} K_r t_1^2 + RC\Delta e_1 + \frac{1}{2} (T - t_1) \Delta e_1] \tag{25}$$

Substituting equations (18), (20), (23), and (24) into (25), and realizing that

$$K + P\ I\ L - \frac{PAL}{2} - \frac{PY}{2} = 0 \tag{26}$$

and

$$t_3 + L + \frac{PT}{2} = - T_d \tag{27}$$

one has

$$\bar{e} = U + VB + W\sqrt{Y+JB} + SB\sqrt{Y+JB} + XB^2 \tag{28}$$

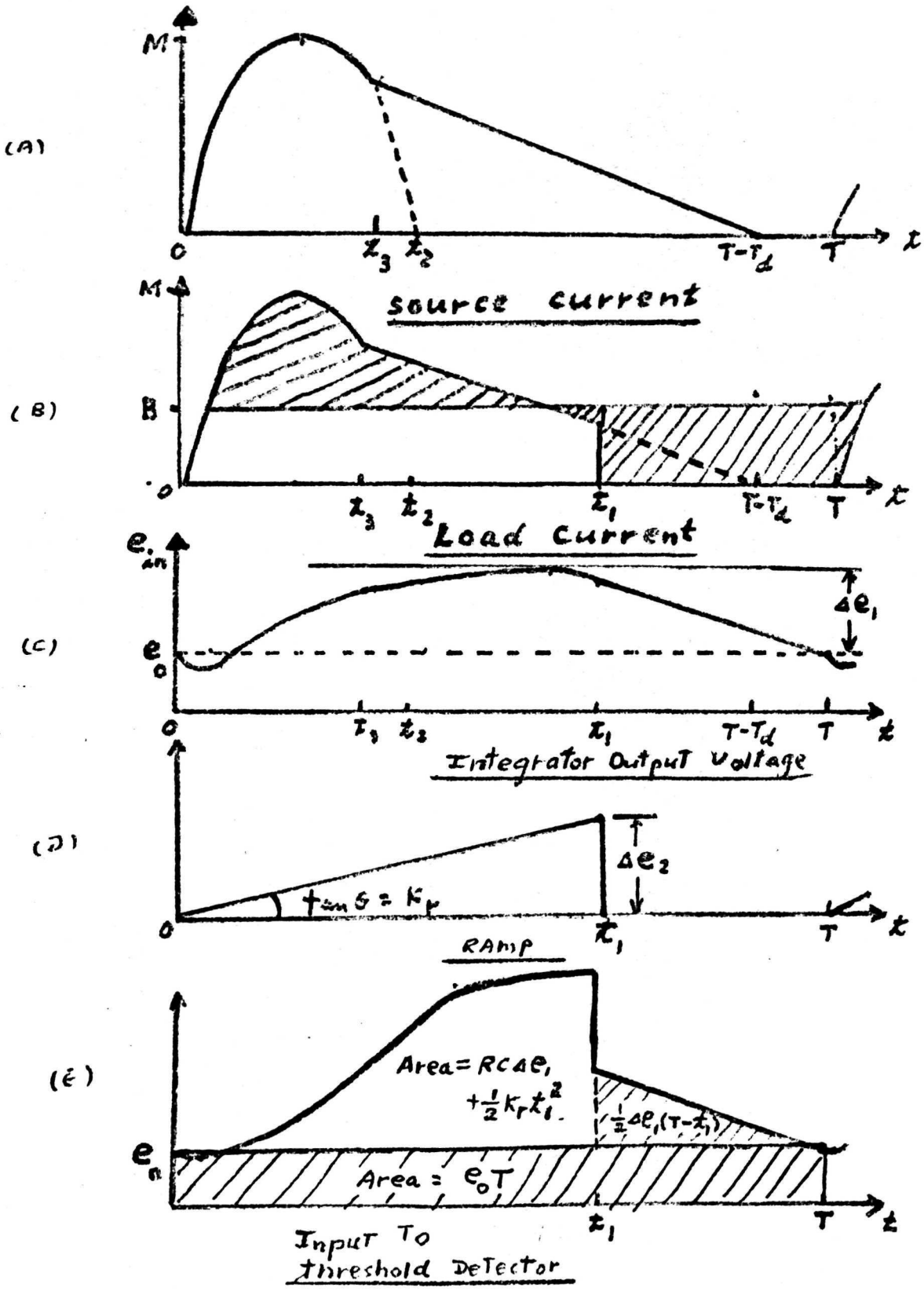


FIGURE 5-32 RELEVANT WAVEFORMS OF SINUSOIDAL SYSTEM

where

$$U = \frac{K_r}{2T}(I^2 + Y - 22T) + \frac{G}{2RCT}$$

$$V = \frac{GY}{2RCT} - GT_d\left(\frac{1}{RC} - \frac{1}{T} - \frac{T_d}{2RCT}\right)$$

$$W = \frac{K_r T_d}{T} \qquad (29)$$

$$S = -G\left(\frac{1}{RC} - \frac{1}{T} - \frac{T_d}{RCT}\right)$$

$$X = -\frac{GJ}{2RCT}$$

Differentiating (28) with respect to B gives

$$\frac{d\bar{e}}{dB} = \frac{2\sqrt{Y+JB}\,(V + 2xB) + WJ + 2SY + 3SJB}{2\sqrt{Y+JB}}$$

Setting (30) to zero results in a third-order equation for B; its nontrivial solution is the particular B at which the system would become unstable. While such a solution can be obtained mathematically, the general influence of the various system parameters on the critical value of B is difficult to interpret. Therefore, a limiting case where t_1 approaches $I=T-T_d$ is considered in order to establish the minimum ramp slope $(K_r)_{min}$ needed to maintain stability throughout the entire on time up to $T-T_d$ of the power switch.

From (18), t_1 approaches I as B approaches -Y/J. Setting (30) to zero therefore gives

$$WJ - SY \cong 0 \qquad (31)$$

Combining (29) and (31) gives

$$K_r = \frac{G\,(PL^2 + 2K)(T-RC-T_d)}{2\,RCT\,T_d} \tag{32}$$

which is equivalent to

$$K_r = \frac{G\,[(T-t_3-T_d)M\,\mathrm{Sin}\,Mt_3 + \frac{2M}{m}\,(1-\mathrm{Cos}\,mt_3)]}{2\,RCT\,T_d} \tag{33}$$

Letting

$$t_3 = dT$$

$$t_2 = cT$$

$$T-T_d = aT$$

$$mt_3 = d\Pi/c$$

$$RC = gT$$

then,

$$(K_r)_{min} = \frac{MG(a-g)[(a-d)\mathrm{Sin}\,\frac{d\Pi}{C} + \frac{2C}{\Pi}\,(1-\mathrm{Cos}\,\frac{d\Pi}{C})\,]}{s(1-a)gT} \tag{34}$$

Equation (34) is the minimum K_r required to maintain stability throughout the variation of on-time up to $t_1=T-T_d$.

As a numerical check, the following parameters are noted from the breadboard design and tests:

$M = 8$	$C = 0.355$	$\mathrm{Cos}\,\frac{d\Pi}{C} = -0.866$
$G = 2.12$	$d = 0.296$	$g = 0.74$
$a = 0.87$	$\mathrm{Sin}\,\frac{d\Pi}{C} = 0.5$	$T = 135\mu s$

Substituting these numbers into (34), one has

$$K_r \cong 0.06\ V/\mu s$$

The K_r actually used in the circuit is

$$K_r = \frac{V_R}{R_r C_r} = \frac{20}{390} = 0.052 \text{ V}/\mu\text{s}$$

and it has been experimentally observed that stability is maintained up to an on-time that is very close to $T-T_d$.

Equation (34), therefore, represents very accurately the minimum slope K_r of the ramp needed to ensure system stability for a fixed input current waveform at a given regulator design.

5.6 Command and Protection System

The command and protection circuitry is contained on five cards. The cards and their functions are as follows:

° Card A; Schematic Figure 5-33

Card A has the input command relays and the undervoltage detector relay driver circuitry. Also the I4 and I5 reference generators are located on this card.

° Card B; Schematic Figure 5-34

Card B has the 5 minute timer circuit.

° Card C; Schematic Figure 5-35

Card C contains the protection circuitry to protect against engine arcs. The V5 and V6 voltage is compared to a reference and if the output voltage is below 90% for 100 milliseconds, three adjustable one-shots are commanded to turn off V4, V5 and V6 as a group, V1 separately and V2 separately.

° Card D; Schematic Figure 5-36

Card D has an I4 current level sensor which senses I4 current and if it is greater than a reference level, it sets a flip-flop turning V9 OFF.

If I4 current is below a different reference level and remains for a fixed time period (5 sec), the flip-flop is reset and V9 turns ON.

° Card E; Schematic Figure 5-37

Card E contains the starting circuit, the overvoltage protection circuit and the undervoltage protection circuit. If the input voltage goes below 180V or exceeds 425V the system is automatically turned OFF.

The command and protection system has been completely integrated into the breadboard and is operating satisfactorily.

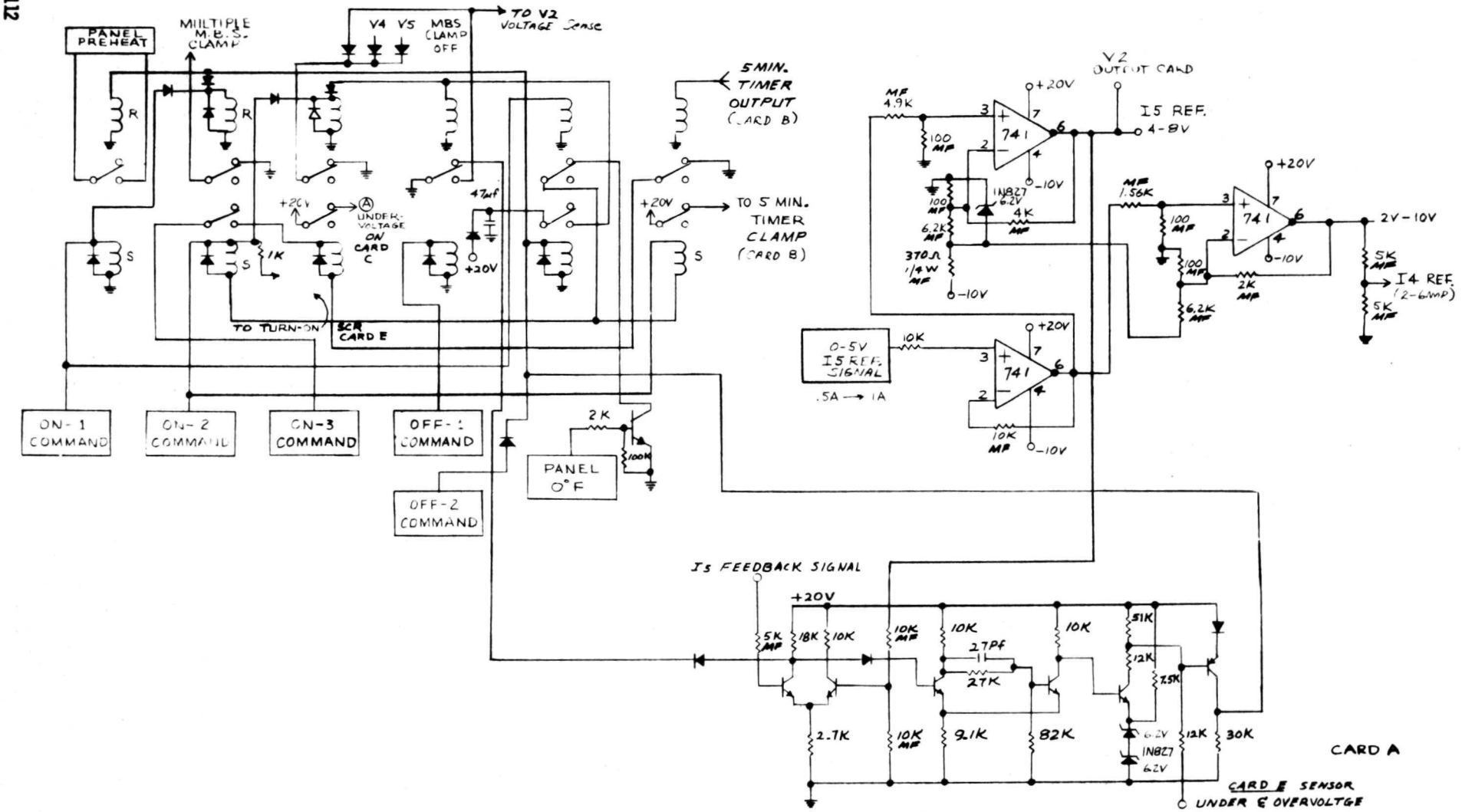
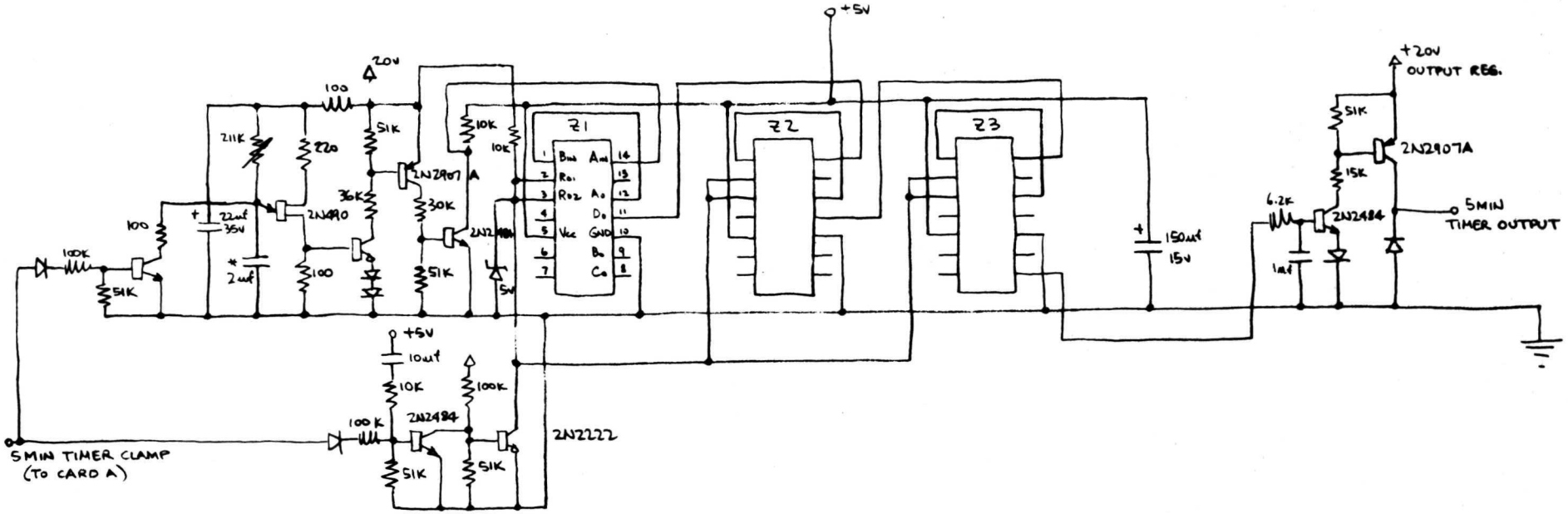


FIGURE 5-33 COMMAND AND PROTECTION SYSTEM SCHEMATIC

5 MIN TIMER CIRCUIT



* 2uf POLYCARBONATE CAPACITOR

Z1, Z2, Z3 USN7493A BINARY COUNTER

CARD B

FIGURE 5-34 COMMAND AND PROTECTION SYSTEM SCHEMATIC

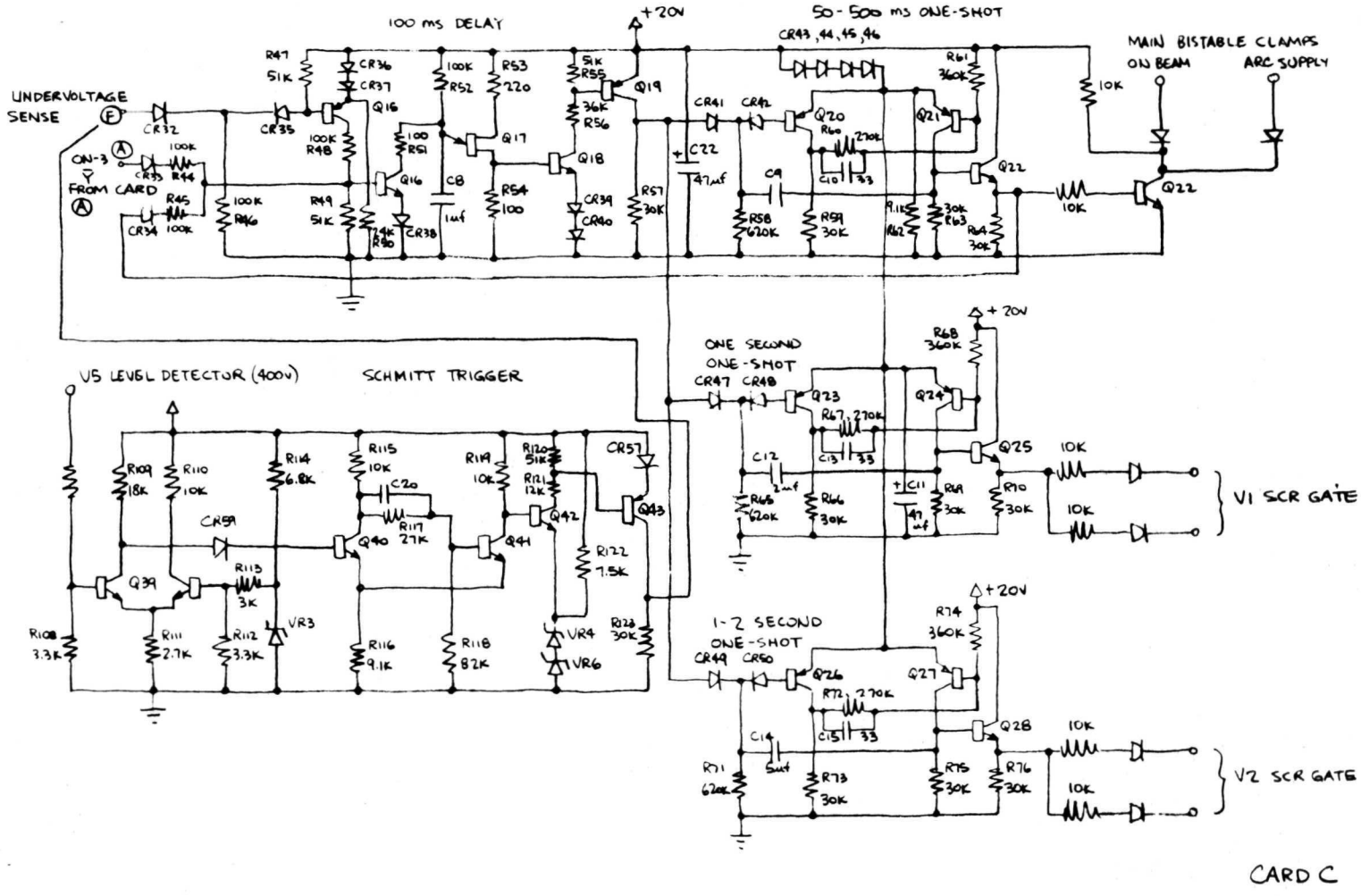


FIGURE 5-35 COMMAND AND PROTECTION SYSTEM SCHEMATIC

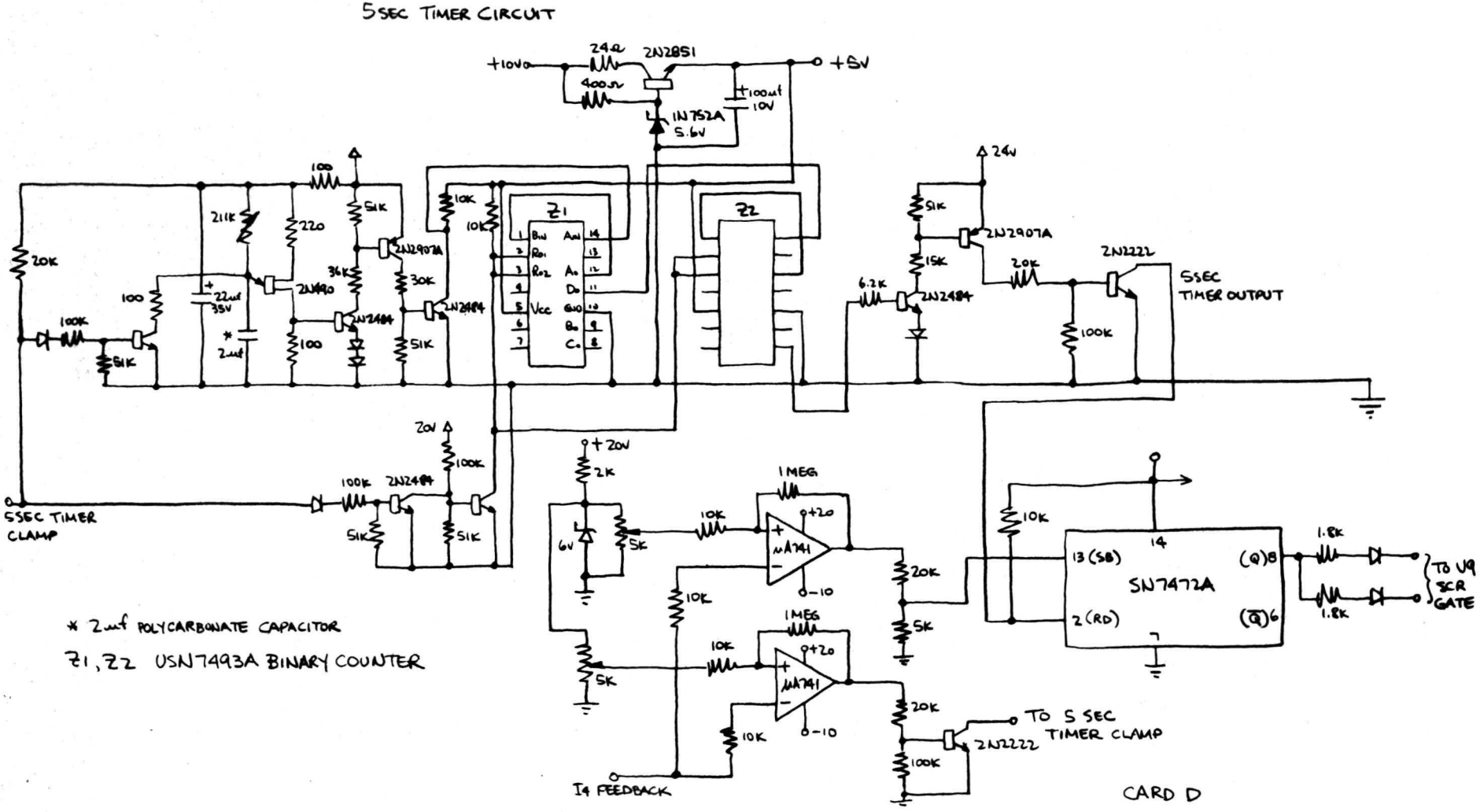


FIGURE 5-36 COMMAND AND PROTECTION SYSTEM SCHEMATIC

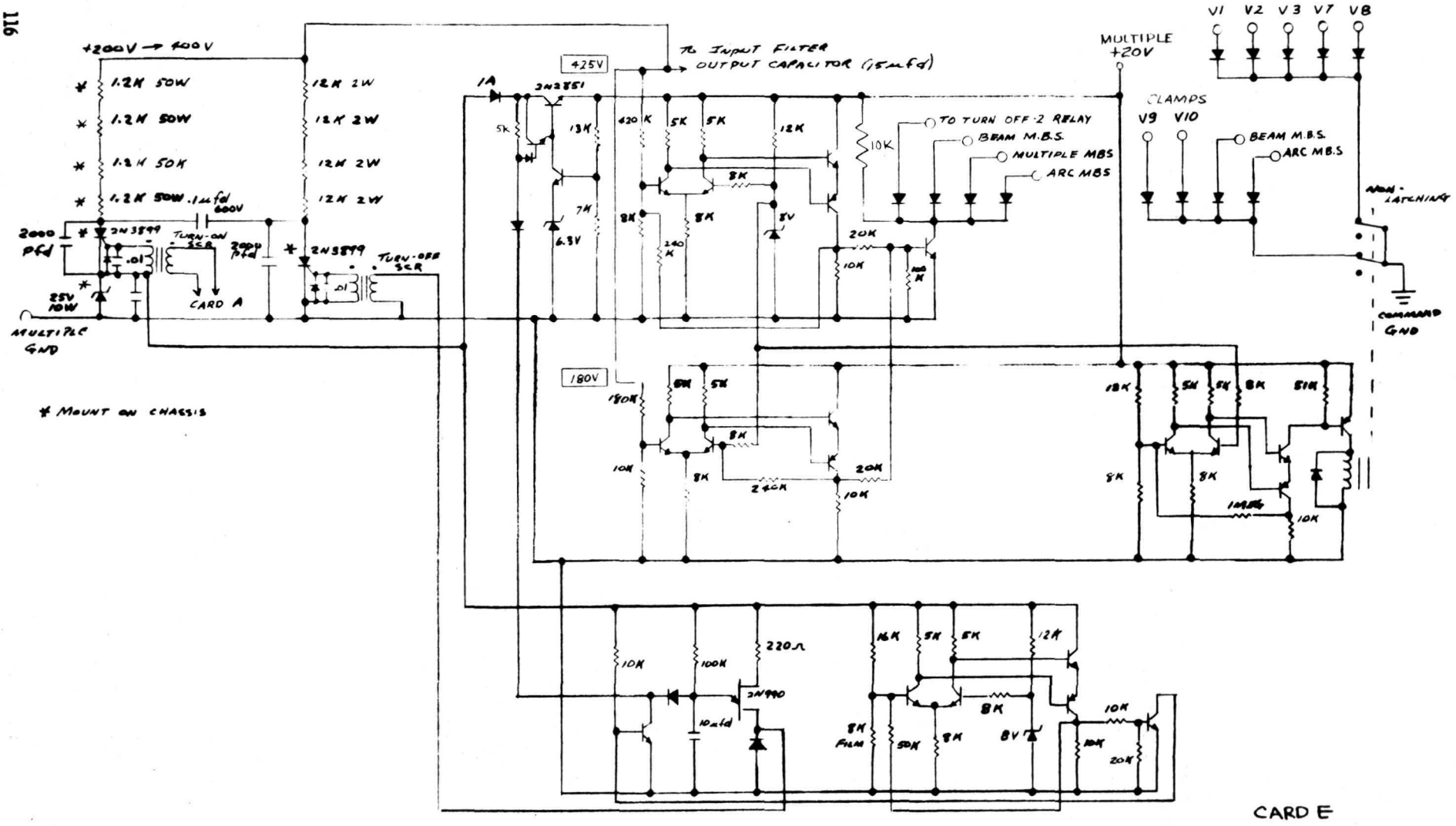


FIGURE 5-37 COMMAND AND PROTECTION SYSTEM SCHEMATIC

5.7 Input Filter

Shown in Figures 5-38 is a schematic of the input filter. It is of a two-stage design, with a resistor connected in series with the capacitor of the first stage to control the resonant peaking of both stages. The second stage is an ordinary LC filter. The filter has to be redesigned to reduce input ripple with half load on the beam and arc supplies.

The second stage capacitance value is 16μfd. It is distributed throughout the breadboard directly at the different inverter inputs so that high AC currents are not circulating throughout the breadboard

INPUT FILTER
FOR
SERIES SCR INVERTER

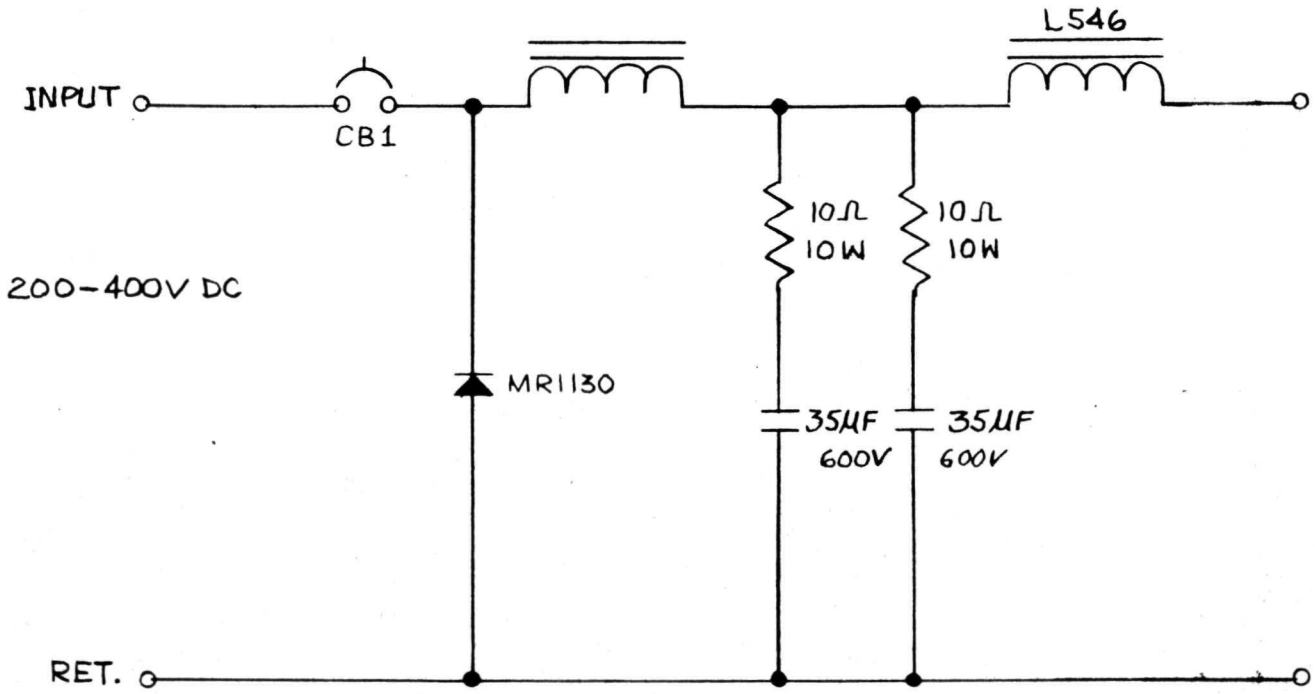


FIGURE 5-38 SCHEMATIC INPUT FILTER

5.8 Integrated Breadboard

The breadboard was constructed into five sub-assemblies:

- input filter
- beam supply
- arc supply
- multiple output inverters and output regulator
- command and protection system.

Figure 5-39 is a photo of the integrated breadboard assembly. Figure 5-40 is a photo of the laboratory facility showing the integrated breadboard and the associated instrumentation and load banks.

Noise problems appeared when integrating the command and protection system into the breadboard which caused false turn-off of the output regulator. Lowering the input impedance of the circuits eliminated the problem.

The V1, V3, V4, V9 and V10 outputs were operated at +2000 Volts potential and no insulation problems were observed.

Figure 5-41 shows the total breadboard efficiency including all internal control power both at full load on all outputs and half load on the beam and arc supplies.

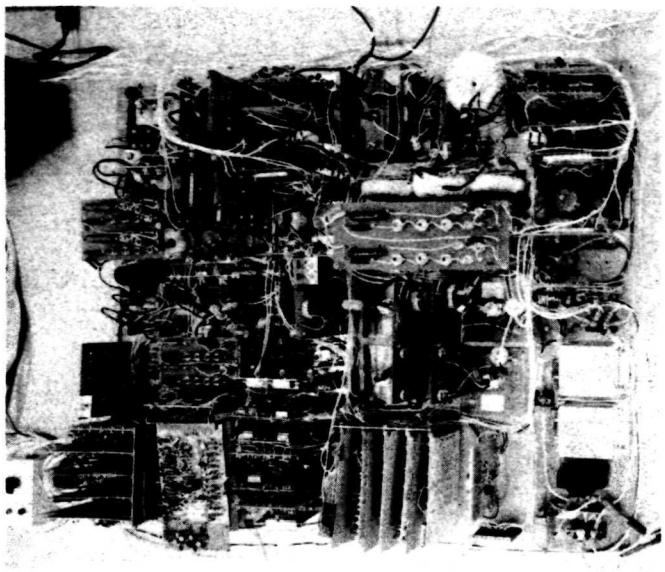


FIGURE 5-39 INTEGRATED BREADBOARD ASSEMBLY

FIGURE 5-40 LABORATORY FACILITY

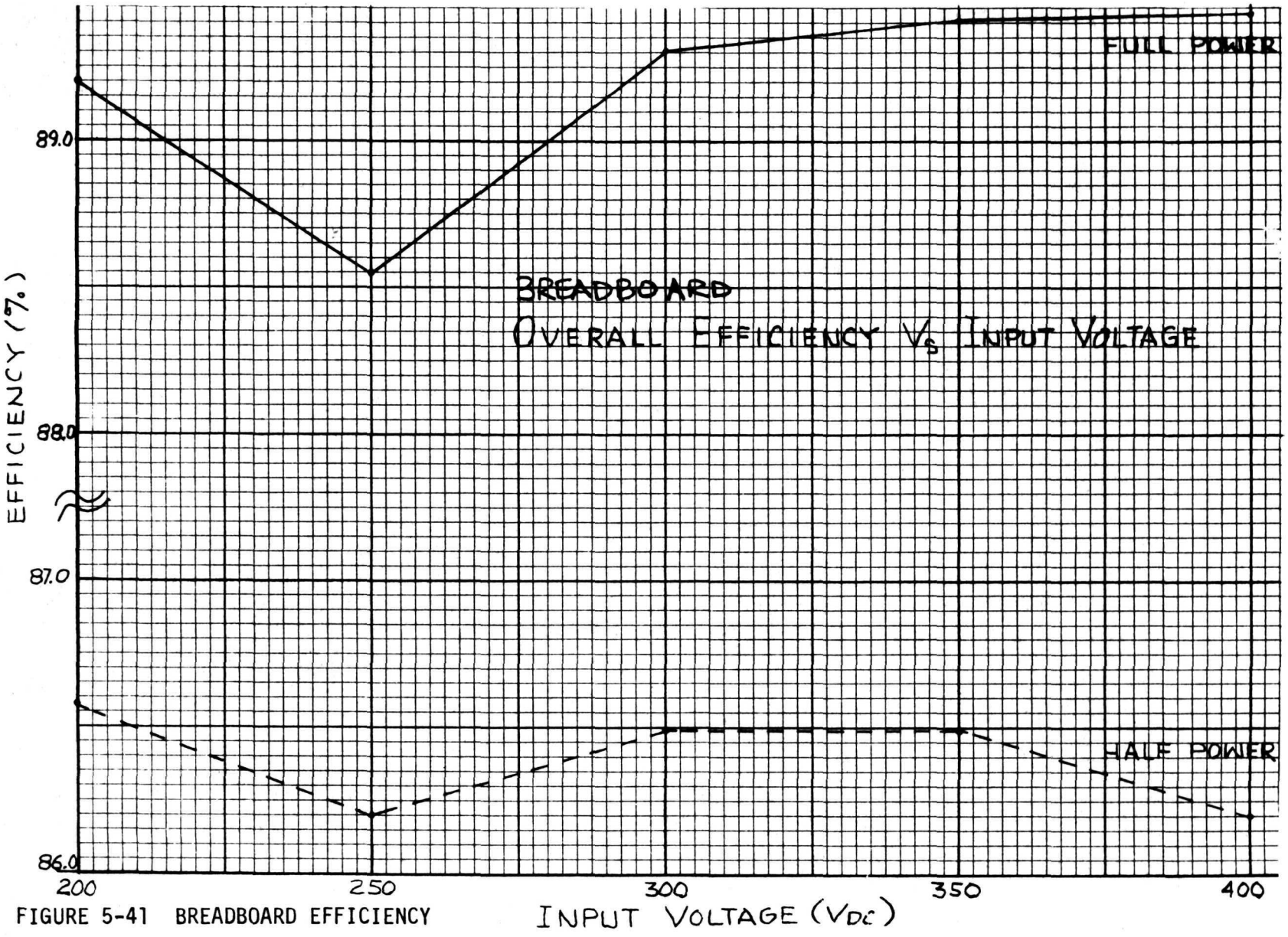


FIGURE 5-41 BREADBOARD EFFICIENCY

Figure 5-42 shows the input ripple as a function of input voltage both at full load and half load. The unit meets specification at full load but is out of specification at half load due to error in performing the filter design. Changing the filter damping factor from + 3db to +12 db, the present filter components would meet specification.

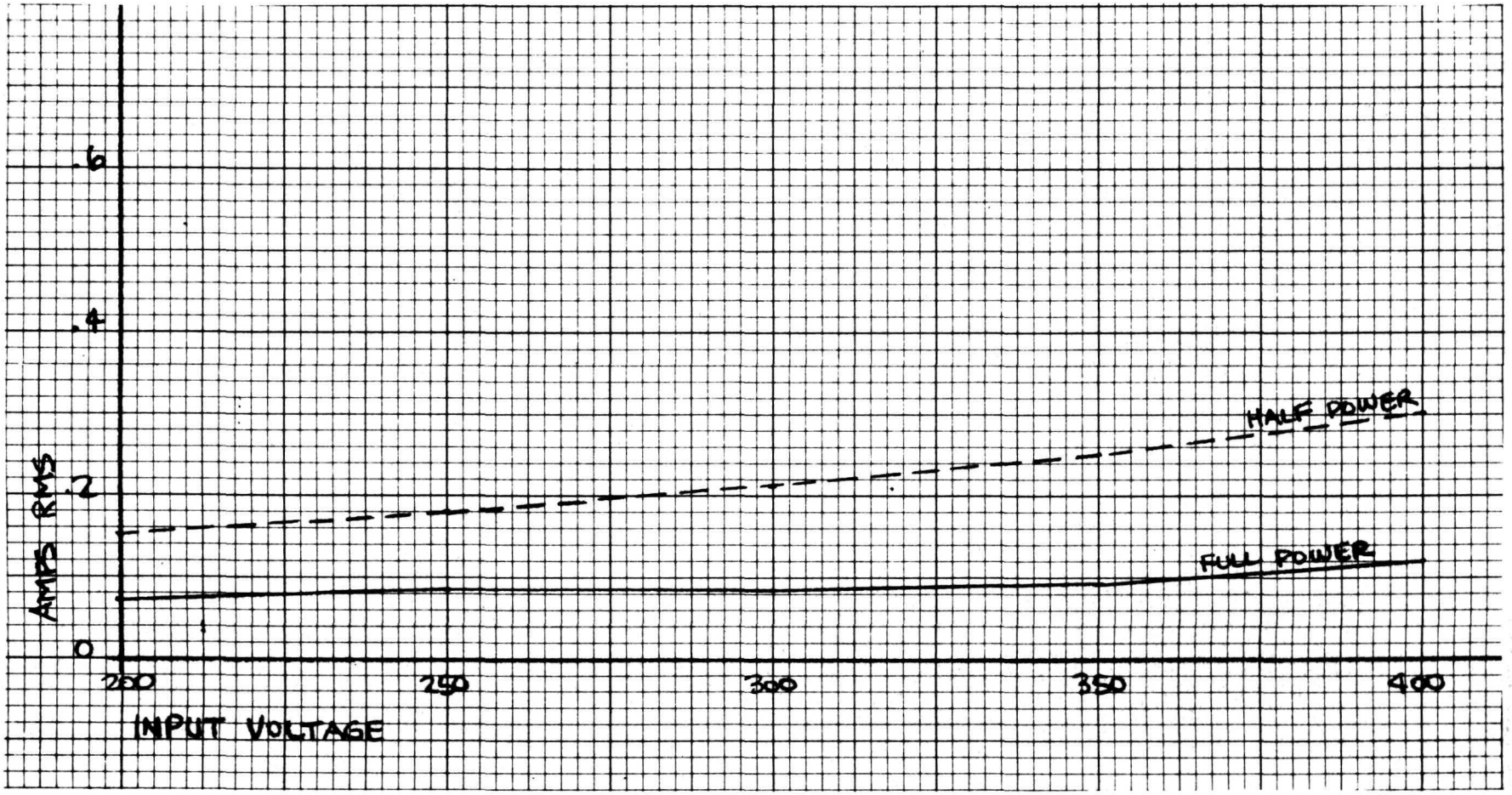


FIGURE 5-42 / BREADBOARD INPUT RIPPLE

6.0 COMPONENTS

6.1 CAPACITORS

A number of dielectrics have been considered for the series resonant capacitors. These include mylar, paper mylar, polystyrene, teflon, mica, polycarbonate, polysulfone, and polypropolene. Mylar and paper mylar are not suitable because of high comparative dissipation factors. Polystyrene has a temperature limitation which makes it unsuitable for internal rise over the +70°C mounting plate. Teflon is questionable because of corona deterioration. Mica and special mica materials have not been promising due to high dissipation factors. Polysulfone is still too recent a development to have performance data. Polycarbonate and polypropolene both are apparently useful, with polypropolene the more attractive of the two because of both its lower DF and, flat DF versus both frequency and temperature (although it is not rated at quite as high in temperature).

The multiple output inverter breadboard utilized reconstituted mica for the series resonant capacitors. The mica dielectric capacitors became so hot that operation was limited to five minute periods. These units were replaced with polypropolene samples and they did not show observable temperature rise for any period of operation.

The first models of the series resonant capacitors (polypropolene) that were delivered experienced shorts after operating in the circuits for some time. The failures may have been as a result of over-stressing the capacitors. Additional insulation was designed into the capacitor and then oil-filled. After this redesign no further failure of the series resonant capacitors occurred.

Because of the 400V input, tantalum capacitors could not be used reliably for the input filter design. New capacitor designs were made for the first stage input filter capacitor using polypropolene.

6.2 MAGNETICS

Magnetics losses in the series inverter were determined both experimentally and analytically. To determine magnetics losses experimentally, calorimeters were used and the temperature rise of the magnetic was measured as it was operating in the inverter. Then dc power was substituted to the magnetic device to obtain the same temperature rise as the dc power supplied is equivalent to the loss in the magnetic when operating in the inverter. Table 6-1 shows the calculated losses and measured losses.

TABLE 6-1
MAGNETICS LOSSES

MAGNETIC TYPE	CALCULATED LOSSES WATTS	MEASURED LOSSES WATTS
BEAM TRANSFORMER	22.53	23.1
BEAM INDUCTOR (SINGLE)	8.41	7.2
BEAM INDUCTOR (CENTER-TAP)	14.28	15.9
ARC TRANSFORMER	6.67	10.3
ARC INDUCTOR (SINGLE)	2.37	1.65
ARC INDUCTOR (CENTER-TAP)	3.55	3.05

The losses in the arc transformer were higher than calculated. Because of the many parallel strands of wire for the high current secondary wire, high circulation currents were present and increased through copper loss. Further development work is required to reduce the losses.

In performing the weight and loss analysis, the series inductors and power transformers contributed to a large percentage of the overall weight and losses. A further investigation was started on the use of ferrites. Development models have to be made to prove the feasibility and determine actual loss and weight improvements.

6.3 SILICON CONTROLLED RECTIFIERS

Table 6-2 forms a brief specification sheet for the ion thruster power processor power SCR's. The main parameters for operation are:

- Peak forward blocking voltage, V_{FOM} (repetitive): listed as desired 800V rating for 550V repetitive circuit conditions.
- Peak reverse blocking voltage, V_{ROM} (repetitive). This is listed as a desired 400V rating for a 250V repetitive circuit condition.
- Turn off time, t_{off}. This must be 10 ms or less for any condition of device temperature or load.

Other parameters which are of vital importance because of their impact on circuit efficiency are:

- Dynamic forward "on" voltage V_F(Dynamic). SCR devices take literally tens to hundreds of microseconds to reach steady-state values after being switched "on." Since the circuit operates with switch "on" periods of about 40 ms, it is obvious the devices must reach near steady values within the first few microseconds if circuit efficiency is to be maintained.

- Forward voltage application rate, dv/dt. This parameter determines the values of the RC suppression network and the selection of the series inductor configuration.

- Gate pulse requirements. All manufacturer's advise that a rapid rise of gate pulse is essential, preferably within 200 ns. For best efficiency, where available pulse energy is limited, one manufacturer recommends for its product a high gate pulse current for a short period, such as 0.5 to 1.0A for the 0.5-1.0μs rather than, say, 400ma for 3μs.

- Stored charge, $Q_{RECOVERY}$. This parameter is indicative of the speed of recovery of the device. It affects the circuit by discharging the capacitor after it has been commutated "off" by the auxiliary SCR. The drop in the capacitor voltage is energy expended in losses and is energy not available for the load although "sensed" as available.

- Current application rate, dI/dt. The dI/dt rating will determine if an inductor is required in series with the auxiliary SCR for limit and control.

- Holding current, I_H. This parameter must be characterized in order to design SCR gate pulse drive circuitry and current sensors for the auxiliary SCR's.

A testing program for SCR's was setup to determine which SCR's were suitable for the series inverter. Test circuit shown in Fig. 6-1 was used to measure the SCR's turn-on characteristic and also the value of the forward ON voltage. The LC values were selected to produce the rated peak current without requiring high V_{cc} input voltage. By this method high static voltages were not present on the SCR which would cause measurement error in the scope in determining the turn-on voltage transient.

SCR TEST CIRCUIT FOR TURN-ON AND
SATURATED DROP CHARACTERISTICS

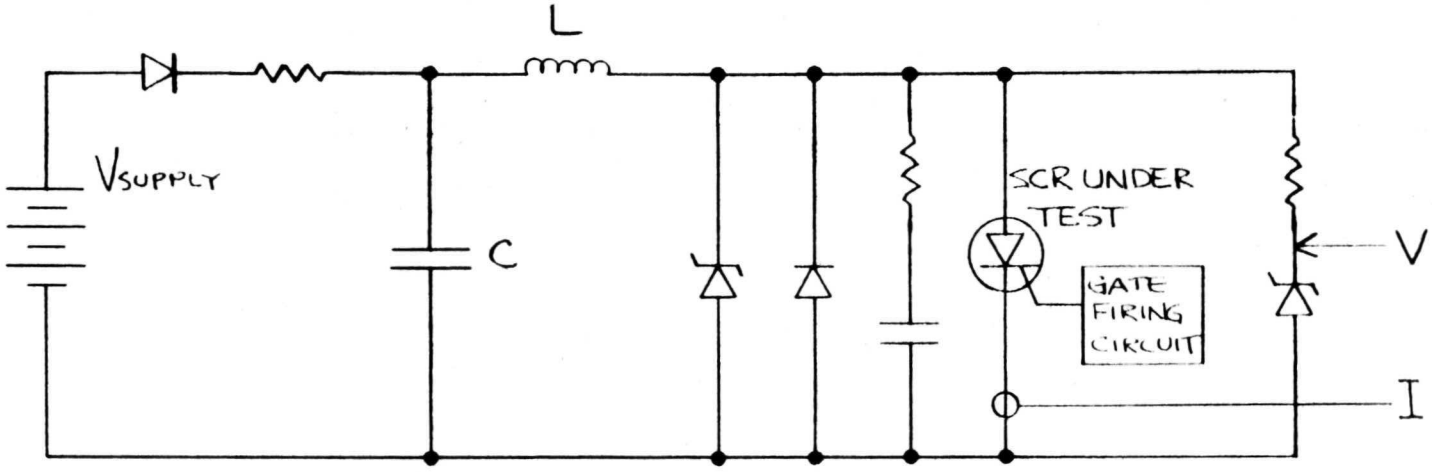


FIGURE 6-1 SCR TEST CIRCUIT

TABLE 6-2

SILICON CONTROLLED RECTIFIER REQUIREMENTS

	HIGH POWER		LOW POWER		
	Main	Auxiliary	Main	Auxiliary	Remarks
$V_{FOM\ (rep)}$ (V)	800 (550)[1]	400 (250)[1]	800 (550)[1]	400 (250)[1]	
$V_{ROM\ (rep)}$ (V)	400 (250)[1]	700 (450)[1]	400 (250)[1]	700 (450)[1]	
I_{PK} (A)	57 (71)[2]	52 (65)[2]	9.3 (11.7)[2]	8.5 (10.6)[2]	
I_{RMS} (A)	24.4	15.2	4.02	2.5	
I_{AV} (A)	13.5	6.79	2.22	1.12	
V_F (V)	<1.5	<2	<1.5	<2	Low as possible
t_{OFF} (μs)	<10	<10	<10	<10	Low as possible
dv/dt (V/μs)	>300	>300	>300	>300	
$V_{F\ (dyn)}$ (V)	5V, 5μs, 150A	5V, 5μs, 150A	5V, 5μs, 25A	5V, 5μs, 25A	Fast switching and low losses
Gate Pulse[4]	2A, 5μs	2A, 5μs	0.4A, 2μs	0.4A, 2μs	
Q_{RCVY}	10 μcoul	See note 3	2 μcoul	See note 3	Low as possible
dI/dt (A/ s)	>100	>100	>100	>100	Not critical
I_H (mA)	<200	100 <I_H <200	<25	25 <I_H <50	
Temp. Range(case)		-20°	to +71°C		

Notes:
1. Actual circuit voltage
2. Short circuit peak current (fault condition can occur less than 0.1% of time).
3. Parameter of secondary importance, supplier please advise.
4. Efficiency requires gate pulse to not be excessive through effective for low $V_{F\ (dyn)}$.

The following SCR devices were tested:

- Type A, 800V, 35A
- Type B, 600V, 35A
- Type C, 550V, 100A
- Type D, 1000V, 110A
- Type E, 600V, 110A
- Type F, 600V, 110A
- Type G, 800V, 110A
- Type H, 800V, 110A

The Type A and B units are the 35A units and were being evaluated for the arc and multiple output inverters.

The lower forward drop, faster turn-on and the higher blocking voltage (800V) for the Type A SCR makes it the best selected for the particular needs of the arc and multiple inverter. The remaining SCR's are 110A units and are being evaluated for the beam supply.

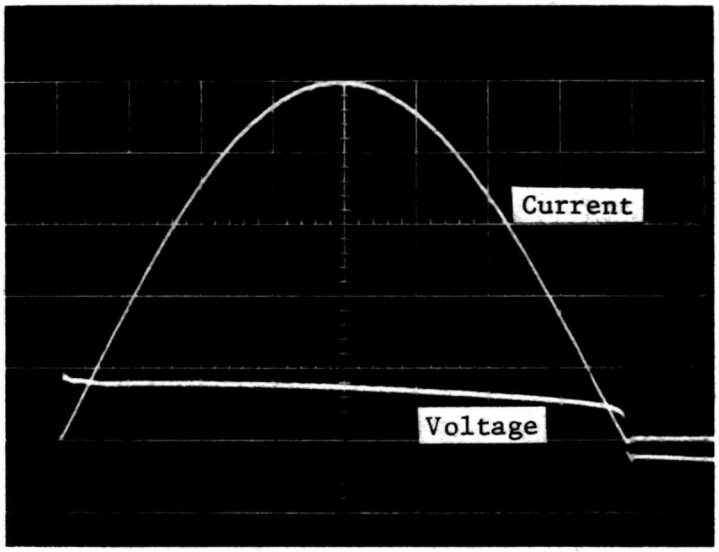
The Type H unit is selected for the main line operation in the beam inverter because of its high blocking voltage rating (800V). Lower forward and saturated drop characteristics would improve inverter operating efficiency.

The Type C device is the best of the high current units but it has low blocking voltage rating (550V). The Type C unit is used as an auxiliary SCR which does not require high blocking voltage.

Actual photo of the main line and auxiliary SCR's for the beam, arc and multiple are shown in Section 5.3, 5.4 and 5.5.1 respectively.

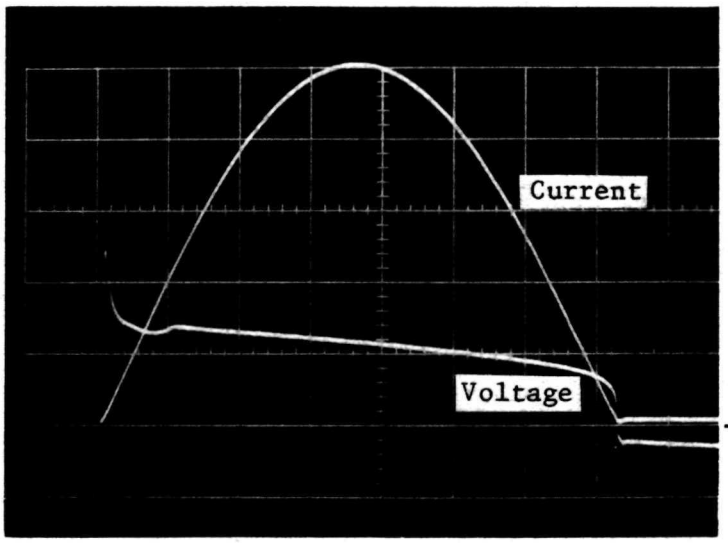
It can be noted from Fig. 6-2 to 6-5, the forward saturated drop is high (approximate 2Vdc) at the peak forward current which will account for the lower efficiency for the SCR inverter power stage.

It is expected that with the test circuit and new SCR's with inter-digitaled construction that the losses will be lowered and efficiency improved.



SEMICON SCRF 168F

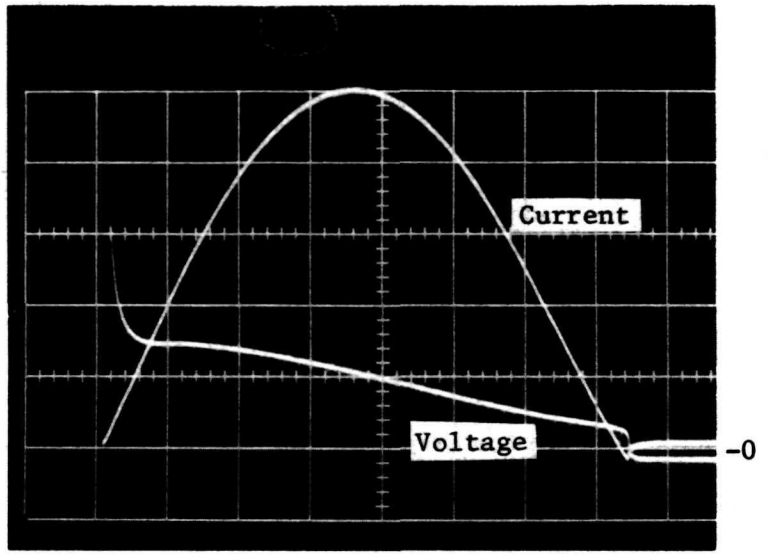
VOLTAGE = 2V/CM
CURRENT = 2A/CM
TIME = 5μs/CM



RCA 60471

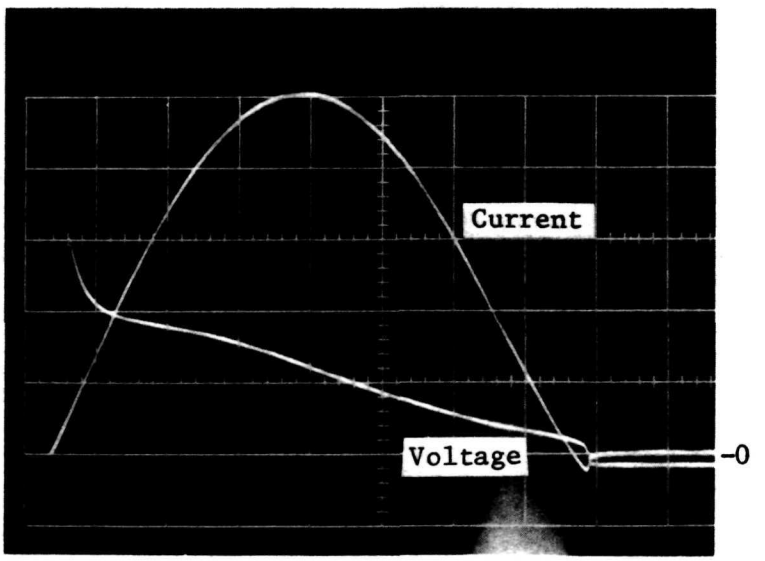
VOLTAGE = 2V/CM
CURRENT = 2A/CM
TIME = 5μs/CM

Figure 6-2 SCR V-I Waveforms



GE C156E

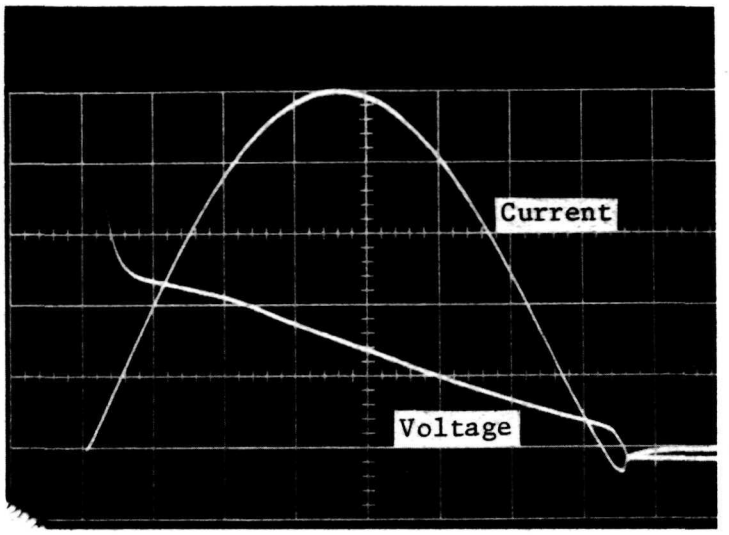
VOLTAGE = 2V/CM
CURRENT = 10A/CM
TIME = 5μs/CM



GE C158P

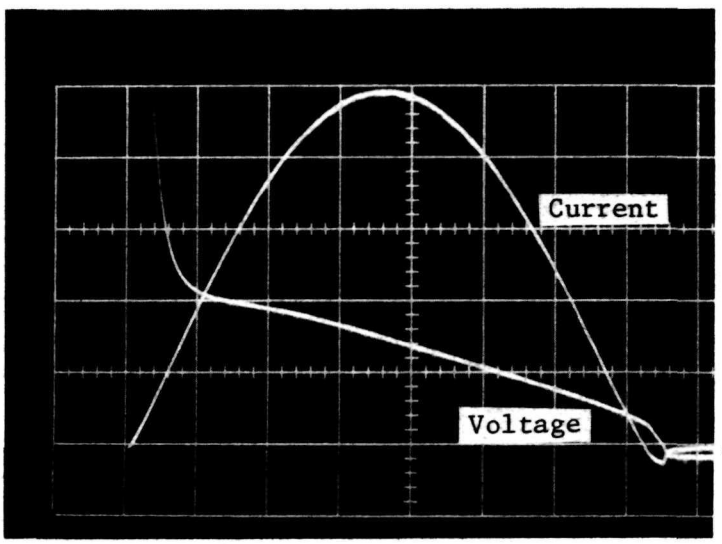
VOLTAGE = 2V/CM
CURRENT = 10A/CM
TIME = 5μs/CM

Figure 6-3 SCR V-I Waveforms



NATIONAL 156M

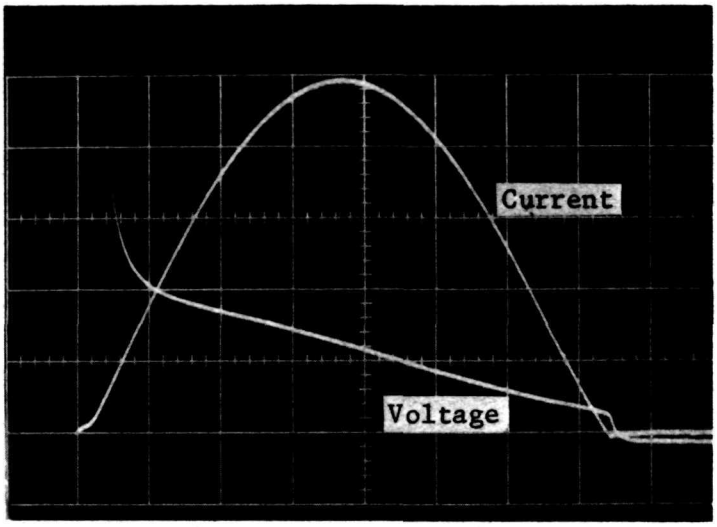
VOLTAGE = 2V/CM
CURRENT = 10A/CM
TIME = 5μs/CM



NATIONAL
ACCELERATED GATE
156M

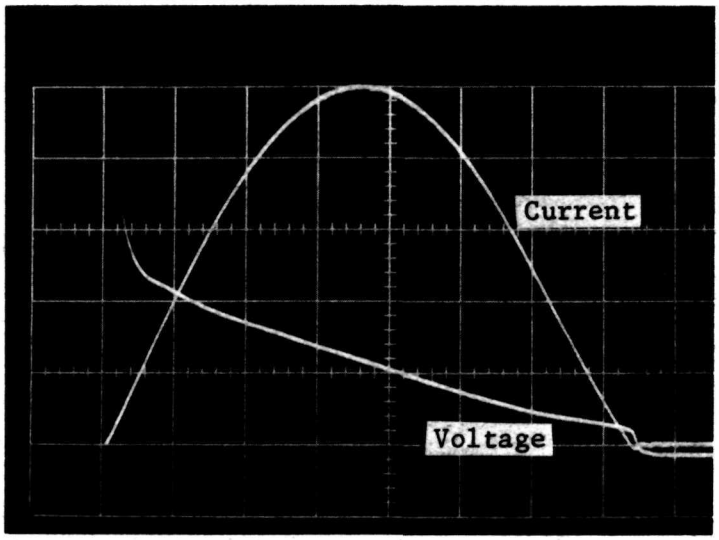
VOLTAGE = 2V/CM
CURRENT = 10 A/CM
TIME = 5μs/CM

Figure 6-4 SCR V-I Waveforms



INTERNATIONAL
RECTIFIER
78-4718

VOLTAGE = 2V/CM
CURRENT = 10A/CM
TIME = 5μs/CM



WESTINGHOUSE 2501P45

VOLTAGE = 2V/CM
CURRENT = 10A/CM
TIME = 5μs/CM

Figure 6-5 SCR V-I Waveforms

7.0 MECHANICAL DESIGN

Figure 7-1 Layout of Power Processor breadboard shows the relative location of each subcircuit and the relative maximum power losses. The basic layout should be useful when designing an engineering model. The control signal lines and the power lines should be isolated from each other so as to eliminate any pick-up problem. One possible solution would be to have power lines on one side and the control signal lines on the other side of the chassis using the chassis as a shield.

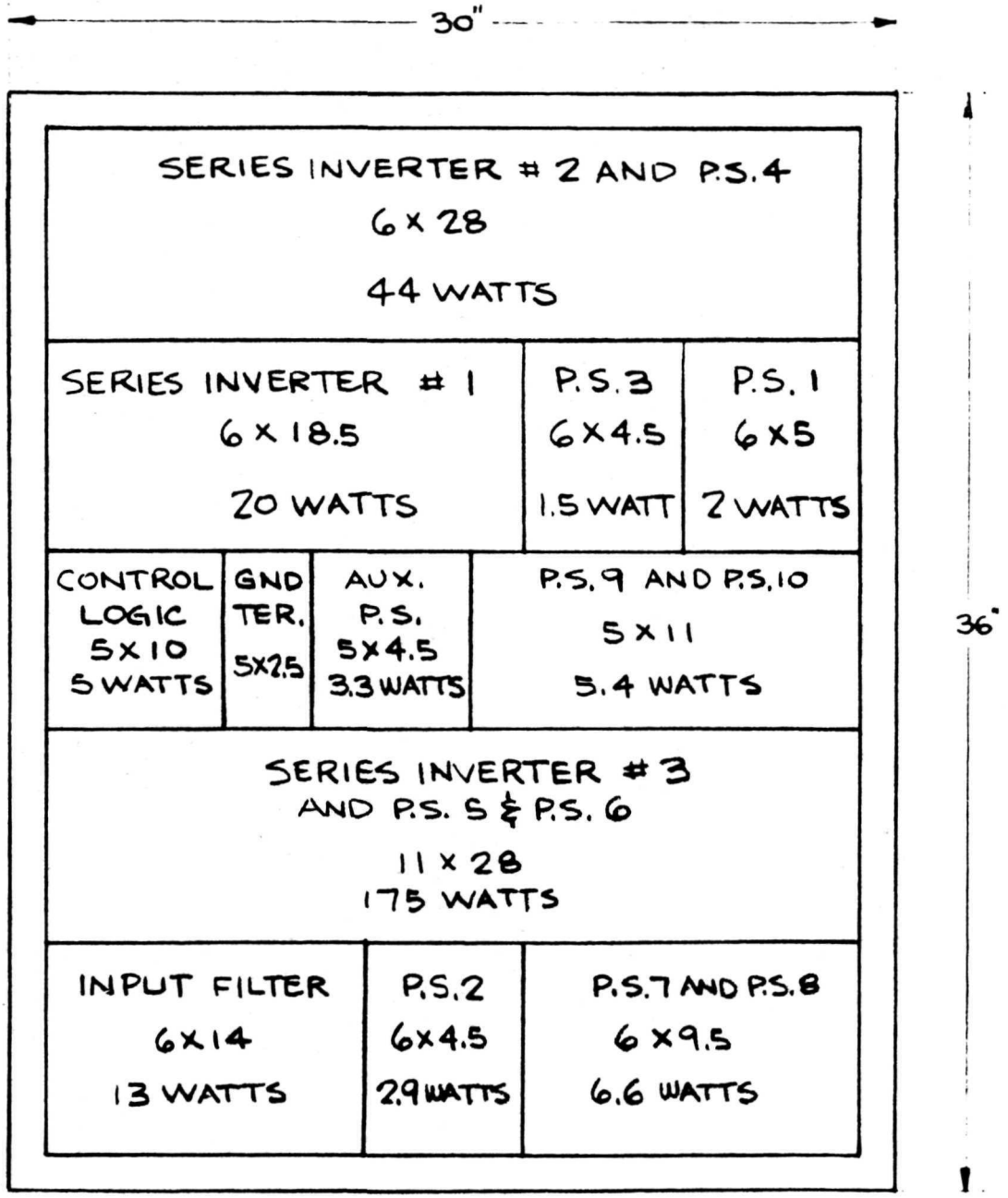


FIGURE 7-1 LAYOUT OF POWER PROCESSOR BREADBOARD

8.0 EFFICIENCY, WEIGHT AND PART COUNT ANALYSIS

8.1 Efficiency Analysis

In order to improve efficiency, a detail investigation must be made of all the losses that are present in the power processor.

Table 8-I lists the losses of the beam supply at maximum load and 250 volt dc input. The main losses occur in the SCR's and magnetics.

Table 8-II lists the losses of the arc supply at full load and at 250V dc input. The magnetics and output diodes are the principle losses. The SCR's are reduced because of the use of Semicon SCR with their fast turn-on and low forward drop.

Table 8-III lists the losses in the multiple output inverter and the output circuit at maximum load and 250 Volt dc input. The main loss occurs in the series inductors and the feedback transformer and clamp transistors.

Table 8-IV lists all the losses in the SCR control logic, the transformer bias driver and the output regulator cards. The total losses are 44 watt which is 2% of the total output power and reduces the overall breadboard efficiency.

Table 8-V summarizes all the power losses and determines the total breadboard efficiency which is 89%. These lists of losses are not the optimum values that can be obtained, but are used as a guide to identify problem areas for further development work.

TABLE 8-I

BEAM SUPPLY LOSSES

	WATTS	PERCENT
Main SCR	82.0	3.75
Auxiliary SCR	33.5	1.53
Transformer	23.1	1.06
Inductors	30.3	1.38
Output Diodes	6.0	0.27
Input Filter	10.0	0.46
TOTAL	184.9 Watts Loss	

Output Power = 2000.0 Watts

Input Power = 2184.9 Watts

Efficiency = $\frac{2000}{2184.9}$ X 100 = 91.3%

TABLE 8-II

ARC SUPPLY LOSSES

	WATTS	PERCENT
Main SCR	5.90	1.34
Auxiliary SCR	1.40	0.32
Transformer	10.30	2.34
Inductors	10.90	2.48
Output Diodes	9.80	2.22
Output Capacitors	1.89	0.43
TOTAL	40.19 Watts Loss	

Output Power = 400.00 Watts

Input Power = 440.19 Watts

Efficiency = $\frac{400}{440.19}$ X 100 = 90.5%

TABLE 8-III

MULTIPLE SUPPLY LOSSES

OUTPUT	OUTPUT POWER (WATTS)	POWER LOSS IN OUTPUT DIODE (WATT)	POWER LOSS IN TRANSFORMER (WATT)	POWER LOSS IN OUTPUT CAPACITOR WATT
V1, 19V	16	0.7	0.7	0.2
V2, 10V	20	1.6	0.9	0.4
V3, 17V	17	0.8	0.6	0.2
V7, 12V	45.6	3.0	1.5	0.8
V8, 22V	11	0.4	0.6	0.2
V9, 12V	36	2.4	1.1	0.6
V10, 22V	13.2	0.5	0.6	0.2
Vaux, 20V	40	1.1	1.5	0.7
TOTAL	198.8	10.5	7.5	3.3

Loss in Output Circuitry 21.3 Watts

Loss in shorting SCR 3.6 Watts

MULTIPLE INVERTER	WATTS	PERCENT
Main SCR	3.6	1.5
Auxiliary SCR	0.84	0.35
Inductors	4.80	2.0
Transistors/Diode	3.12	1.3
Feedback Transformer	7.20	3.0

Total Losses = 44.46

Input Power = 243.26

$$\text{Efficiency} = \frac{198.8}{243.26} \times 100 = 81.6\%$$

TABLE 8-IV

CONTROL CIRCUITS

SCR CONTROL LOGIC	I @ 20V INPUT	POWER	
Card 1 -- Main Bistable & Main Firing Circuit	120 ma	2.4	
Card 2 -- Local Bistable & 10 μsec oneshot	34 ma	0.68	
Card 3 -- Capacitor Sensor & Auxiliary Firing	177 ma	3.54	
Card 4 -- Current Sensor	40 ma	0.80	
TOTAL	371 ma	7.42	
(for three inverters) (X3)			22.26
REGULATOR CARDS			
Beam Supply	66 ma	1.32	
Arc Supply	38 ma	0.76	
Multiple Output	225 ma	4.50	
2 KHz Inverter	30 ma	0.60	
TRANSFORMER BIAS DRIVER			
Beam	310 ma (OFF) 30 ma (ON)	6.20	
Arc	230 ma (OFF) 200 ma (ON)	4.60	
Multiple	192 ma	3.82	
	TOTAL LOSSES	44.06	

TABLE 8-V

OVERALL SYSTEM EFFICIENCY

	OUTPUT POWER	LOSSES
Beam Supply	2000.0	184.90
Arc	400.0	40.19
Multiple	158.8	44.46
Control circuits		44.06
TOTAL	2558.8 Watts	313.41 Watts

Input Power = 2872.21 Watts

Overall Efficiency = $\frac{2558.8}{2872.21}$ X 100 = 89.0%

8.2 Weight Analysis

The present breadboard design was analyzed to determine the relative weights for each function. Table 8-VI through 8-X identify the electrical components weights and the breadboard mechanical components. The design objective at this time was to demonstrate circuit technology and efficiency but not weight.

Table 8-VI lists the weights of the input filter. The penalty of this design is the filter capacitor weight because of the use of polypropolene instead of tantalum which also caused an increase in the filter inductance value and weight.

Table 8-VII lists the weight of the beam supply. The weight of the magnetics account for a major percentage of the total weight. Higher frequency operation and magnetic redesign should reduce the weight.

Table 8-VIII lists the weight of the arc supply. The major weight is in the magnetics and the control electronics. Magnetic redesign should reduce the magnetic weight and a redesign of the control electronics with integrated circuits will reduce the control electronics weight.

Table 8-IX lists the weight of the multiple output inverter, the output regulators and the command and protection system. The major percentage of the weight is in the magnetics and control electronics and a redesign in these areas will reduce the component weight.

Table 8-X summarizes the total breadboard weight at the present time. Many components are overdesigned at the present time in order to keep the stress levels down and not cause failures. Designing for the 200 to 400 volt dc input source presents many component problems where optimum components are not available and additional development work is going on.

TABLE 8-VI

WEIGHT ANALYSIS - INPUT FILTER

Item	Electrical Components		Mechanical Components	
	gms	lbs	gms	lbs
Input Inductor	658.2	1.45		
Output Inductor	265.3	0.56		
Capacitors - 1st stage	873.0	1.93		
Misc Hardware			200.0	0.44
Subtotal Weights	1787.5	3.94	200.0	0.44
TOTAL of Electrical and Mechanical Components	1987.5 gms		4.38 lbs	

TABLE 8 - VII

WEIGHT ANALYSIS - BEAM SUPPLY

Item	Electrical Components		Mechanical Components	
	gms	lbs	gms	lbs
Transformer - Output	1147.5	2.53		
Capacitors - Series	277.6	0.50		
Inductors - Series	1585.7	3.49	166.8	0.37
Output Capacitors	414.6	0.91		
Input Capacitor	150.4	0.33		
Control Logic	432.5	0.95	206.0	0.45
Connectors			89.5	0.20
SCR's	514.0	1.13		
di/dt Inductors	336.6	0.74		
Current Monitor Transformers	247.5	0.54		
Misc. Transformers	143.5	0.32		
Protection - Cap. Voltage	355.6	0.78		
Suppression Network	133.2	0.29		
Output Circuitry	60.0	0.13		
Fiberglass			992.1	2.19
Heat Sinks			710.0	1.56
Chassis			1820.0	4.00
Misc. Wire & Hardware			900.0	2.00
Subtotal Weight	5798.7	12.64	4884.4	10.77

TOTAL of Electrical and Mechanical Components: 10683.1 gms, 23.41 lbs

TABLE 8 - VIII

WEIGHT ANALYSIS - ARC INVERTER

Item	Electrical Components		Mechanical Components	
	gms	lbs	gms	lbs
Transformer - Output	362.0	0.80		
Inductors - Series	837.9	1.88		
Capacitor - Series	71.2	0.16		
SCR's	42.3	0.09		
Capacitors Output	122.8	0.27		
Diode - Output	70.8	0.16		
Control Electronics	432.5	0.95	206.0	0.45
Connectors			89.5	0.20
Zener Diode Output	16.7	0.04		
Misc. Magnetics	234.6	0.52		
Protection - Cap. Voltage	243.9	0.54		
Chassis			930.0	2.05
Capacitor - Input	70.5	0.16		
Epoxy			202.5	0.45
Bracket			94.8	0.21
Wire & Misc. Hardware			350.0	0.77
Subtotals	2505.2	5.57	1872.8	4.13

TOTAL of Electrical and Mechanical Components 4378.0 gm 9.70 lb

TABLE 8 - IX

WEIGHT ANALYSIS

COMMAND & PROTECTION SYSTEM & MULTIPLE OUTPUT INVERTER

Item	Electrical Components		Mechanical Components	
	gms	lbs	gms	lbs
Inductors	685.6	1.51		
Capacitors - Series	40.5	0.09		
SCR's	42.3	0.09		
Control Electronics	380.8	0.84	164.0	0.36
Connectors			70.8	0.16
Current Transformers	210.0	0.46		
Dummy Transformers	574.8	1.27		
Filter Cap - Input	70.5	0.16		
Power Transistors	72.6	0.16		
di/dt Inductors	109.4	0.24		
Protection Cap. Voltage	243.9	0.53		
Regulators - Output	288.0	0.63	473.6	1.04
Output Circuits	405.0	0.89	630.0	1.39
Output Transformers	1143.6	2.50		
Oscillator Transformer	56.8	0.13		
Storage Cap	122.8	0.28		
Start Circuit	109.7	0.24		
Command Controls	324.0	0.71	206.0	0.45
Plate			2260.0	4.97
Brackets			442.8	0.98
Wire & Misc. Hardware			454.0	1.00
Subtotals Weight	4880.3	10.73	4701.2	10.35

TOTAL of Electrical and Mechanical Components 9581.5 gm 21.08 lb

TABLE 8-X

TOTAL WEIGHT SUMMARY

Item	Electrical Components	Mechanical Components
Input Filter	3.94	0.44
Beam Supply	12.64	10.77
Arc Supply	5.57	4.13
Command & Protection/ Multiple Output Inverter	10.73	10.35
Subtotal Weight	32.88 lbs	25.69 lbs
TOTAL WEIGHT	58.57 lbs	

8.3 Part Count Analysis

The part count for the total integrated breadboard was determined and is shown in Tables 8-XII through 8-XVII. The quantity of each component type is listed with its failure rate per part and the total failure rate. Table 8-XI gives the generic part failure rates for Spacecraft applications and is used in the tables. This table is not meant to give an absolute value of the failure rate for components such as the high power SCR's and series capacitors where no reliability data exist, but is used as a guide to determine overall failure rate if data becomes available.

Table 8-XII lists the input filter data

Table 8-XIII lists the parts included in the SCR inverter control logic

Table 8-XIV lists the parts included in the multiple output inverters, output regulators and the command and protection system.

Table 8-XV lists the parts in the arc supply

Table 8-XVI lists the parts in the beam supply.

Table 8-XVII summarizes the total part count of the present electrical design.

Table 8-XI Generic Part Failure Rates for Spacecraft Applications

Part Type	Failure Rate (Failures/10^9 hrs) at 25 Percent Rated Stress and 30°C Amb. Temp.
Capacitors	
Ceramic	6*
Ceramic, feed-thru filter	10
Glass	3*
MICA	4*
Mylar	20*
Polystyrene	1
Tantalum, solid	9*
Tantalum, foil	20
Variable	40
Connectors	
General	40*
Coaxial	10*
Connector pins (active)	0.1*
Diodes	
Silicon, general purpose	2*
Silicon, power rectifier	44*
Tunnel	100
Varactor	40
Zener	23
4-level device (SCR, etc.)	136*
Inductive Devices	
Inductors (per coil)	10*
Transformers	
(<0.5 w)	14*
(0.5-1 w)	14*
(10-1000 w)	14*
Integrated Circuits	
Analog amplifier	150
RTL	35
DTL	25
TTL	50
MOS	100
Hybrid (Nonmicrowave)	65
Resistors	
Compsition, carbon	2*
Metal film	1*
Wirewound allurate	10
Wirewound power	10
Wirewound variable	50*
Relays	
Magnetic latching	64*
General purpose	106*
Microwave Components	
Diplexer	131
Filters (low pass)	5
Omnimode transducer	3
Hybrid	23
Coupler	13
Variable attenuator	80
Waveguide	1
Waveguide tuning screw	0.5
Ferrite junction	5
Microwave diode	50
Stripline structure	1
Transistors	
Silicon (high power > 10 w)	40*
Silicon (low power <10 w)	10*
Field effect	60
Mechanical Components	
Squib pin puller	300,000/cyc.
Separation nut, explosive	48,000/cyc.
Hold down spring	110
Hold down arm	100
Hold down latch	100
Torsional spring	220
Compression spring	110
Pin puller device	48,000/cyc.
Shear pin	6
Hinge joint	100
Ratchet latch	100
Paddle hinge assembly	662
Boom hinge assembly	600,000/cyc.
Other Components	
Antenna	90
Azimuth motor	200
Bearings	11
Bolometer	620
Compression spring	110
Crystals, quartz	20
Fill	70
Fuse	200
Heater, blanket	14
Heater, strip, flexible	10
Holding latch mechanism	100
Hydraulic damper, viscous	500
Interconnections	
Solar array	1
Soldered	0.5
Welded	0.5
Magnetic amplifier	14
Nozzle, hot gas	166/cyc.
Cold gas	16/cyc.
Pressure transducer	540
Pressure switch	320/hr + 80/cycle
Resolver	100
Slip rings and brushes	860 per brush per slip ring contact
Shuttle or mechanical switch	461
Solar cell	1
Solenoid	347
Squib	300,000/cyc.
Tank (per inch of weld)	0.6
Tanks (propellant)	120
Tank bladder	330
Thermistor	35
Thermostat	70
Thermostat switch	9
TWT (0-5 w)	500
(5-20 w)	2500
(>20 w)	7250

*Based entirely on orbital operating data

TABLE 8 - XII
PARTS COUNT ON INPUT FILTER

Input Filter	Quantity	Failure Rate	Total Failure Rate
Diode	1	44	44
Choke	2	10	20
Resistor	2	10	20
Capacitor	2	20	40
	7	84	124

TABLE 8 - XIII

Part Count for SCR Inverter Control Logic

Card #1 Logic Control	Quantity	FR	Total
Transistor	40	10	400
Diode	65	2	130
Zener	5	23	115
Resistor	93	2	186
Capacitor	26	9	234
Pot.	1	50	50
	230	96	1115
Card #2 Logic Control			
Transistor	18	10	180
Diode	30	2	60
Zener	3	23	69
Resistor	46	2	92
Capacitor	18	9	162
	115	46	563
Card #3 Logic Control			
Transistor	15	10	150
Diode	11	2	22
Zener	4	23	92
Resistor	48	2	96
Capacitor	9	9	81
I. C.	2	50	100
	104	96	541
Card #4 Logic Control			
Pot.	4	50	200
Transistor	6	10	60
Diode	20	2	40
Zener	10	23	230
Resistor	26	2	52
Capacitor	14	9	126
I. C.	2	150	300
	82	246	1008

TABLE 8 - XIV

PARTS COUNT ON OVERALL MULTIPLE OUTPUT INVERTER

MULTIPLE

Power SCR Section	Quantity	FR	Total
SCR	6	136	816
Diode	35	2	70
Zener	7	23	161
Capacitor	16	9	144
Resistor	22	2	44
Transistor	3	40	120
Transformer (Includes Inductors, Current Transformer, Pulse Transformer)	15	14	210
	104	226	1565
V1 Output (19V, .85A)			
SCR	2	136	272
Diode	21	(44) 2	126
Zener	4	23	72
Capacitor	8	9	72
Resistor	40	2	80
Transistor	9	10	90
Transformer	4	14	56
I.C.	4	150	600
Pot	1	50	50
	93	396	1418
V2 Output (10V @ 2A)			
SCR	2	136	272
Diode	18	(44) 2	120
Zener	3	23	69
Capacitor	9	9	81
Resistor	41	2	82
Transistor	9	10	90
Transformer	3	14	42
I.C.	5	150	750
Pot.	1	50	50
	91	396	1556

TABLE 8 - XIV (Continued)

V3 Output (17V @ 1A)	Quantity	FR	Total
SCR	2	136	272
Diode	17	(44)2	118
Zener	4	23	92
Capacitor	7	9	63
Resistor	40	2	80
Transistor	8	10	80
Transformer	3	14	42
I.C.	4	150	600
Pot.	1	50	50
	86	396	1397

V7 Output (12V @ 3.8A)			
SCR	2	136	272
Diode	17	(44)2	118
Zener	4	23	92
Capacitor	9	9	81
Resistor	39	2	78
Transistor	7	10	70
Transformer	3	14	42
I.C.	4	150	600
Pot.	1	50	50
	86	396	1403

V8 Output (20V @ .6A)			
SCR	2	136	272
Diode	21	(44) 2	126
Zener	4	23	92
Capacitor	10	9	90
Resistor	33	2	66
Transistor	8	10	80
Transformer	4	14	56
I.C.	3	150	450
Pot.	1	50	50
	86	396	1282

TABLE 8 - XIV (Cont.)

V9 Output (12 V @ 3 A)	Quantity	FR	Total
SCR	2	136	272
Diode	16	(44) 2	116
Zener	3	23	69
Capacitor	9	9	91
Resistor	33	2	66
Transistor	8	10	80
Transformer	3	14	42
I. C.	3	150	450
Pot.	1	50	50
	78	396	1236
V 10 Output (20 V @ .6 A)			
SCR	2	136	272
Diode	21	(44) 2	126
Zener	4	23	72
Capacitor	10	9	90
Resistor	33	2	66
Transistor	8	10	80
Transformer	4	14	56
I. C.	3	150	450
Pot.	1	50	50
	86	396	1262
Aux. Output and Telemetry Inverter			
SCR	2	136	272
Diode	20	(44) 2	124
Zener	3	23	69
Capacitor	9	9	81
Resistor	31	2	62
Transistor	10	10	100
Transformer	4	14	56
I. C.	2	150	300
	81	346	1064

TABLE 8 - XIV (Cont.)

Card A Command Logic	Quantity	FR	Total
Transistor	7	10	70
Diode	18	2	36
Zener	3	23	69
Resistor	34	2	68
Capacitor	1	9	9
Relay	6	64	384
I. C.	3	150	450
	72	260	1086
Card B Command Logic			
Transistor	9	10	90
Diode	6	2	12
Zener	1	23	23
Resistor	20	2	40
Capacitor	5	9	45
I. C.	3	150	450
Pot.	1	50	50
	45	246	710
Card C Command Logic			
Transistor	21	10	210
Diode	27	2	54
Zener	3	23	69
Resistor	54	2	108
Capacitor	7	9	63
	112	46	504
Card D Command Logic			
Pot.	3	50	150
Transistor	12	10	120
Diode	7	2	14
Zener	2	23	46
Resistor	38	2	76
Capacitor	3	9	27
I. C.	3	150	450
	68	246	883

TABLE 8 - XIV (Cont.)

Card E Command Logic	Quantity	FR	Total
Transistor	23	10	230
Diode	20	2	40
Zener	4	23	92
Resistor	55	2	110
Capacitor	6	9	54
Transformer	2	14	28
SCR	2	136	272
Relay	1	64	64
	113	260	890
Multiple Output Current Source			
Transistor	1	10	10
Zener	1	23	23
Resistor	4	2	8
Capacitor	1	9	9
	7	44	50

Output V_1, V_2, V_3, V_7, V_8, V_9, V_{10}, Aux,	=	687
Logic Control Card # 1, 2, 3, 4	=	531
Command Logic Card A, B, C, D, E	=	410
Current Source	=	7
Power Stage	=	104

TABLE 8 - XV

PARTS COUNT ON ARC SUPPLY

V4 Control Amp		Quantity	FR	Total
Transistor		7	10	70
Diode		23	2	46
Zener		5	23	115
Resistor		28	2	56
Capacitor		8	9	72
Transformer	Output Transformer Included	5	14	70
I. C.		4	150	600
		80	210	1029

Power Stage	100
Logic Control Card # 1, 2, 3, 4	531
Current Source	7
	718

TABLE 8 - XVI
PARTS COUNT ON BEAM SUPPLY

V5 & V6 CONTROL	Quantity	FR	Total
Transistor	12	10	120
Diode	29	2	58
Zener	8	23	184
Resistor	48	2	96
Capacitor	9	9	81
I. C.	7	150	1050
Transformer	10	14	140
Pot.	2	50	100
	125	260	1829

Power Stage	101	
Include Input Cap	1	
Include Transformer	1	
Include Output Diode	8	
Include Output Cap.	2	
Total		113
Logic Control Card # 1, 2, 3, 4		531
Current Source		7
Total		776

TABLE 8 - XVII

PARTS COUNT ON TOTAL SYSTEM (ERC)

	Part Count Total	Failure Rate Total	Total Failure Rate
MULTIPLE	1,739	4930	19533
ARC	718	694	4256
BEAM	776	744	5056
INPUT FILTER	7	88	124
	3,240	6456	28969

9.0 TEST EQUIPMENT

Four different load banks were constructed to act as loads for the ion engine power processor outputs:

- Beam supply load
- Arc supply load
- Multiple output loads operating at + 2000 VDC
- Mulitple output loads operating at ground

These load banks were constructed to facilitate testing of the power processor and to provide safety by shielding the high voltage from laboratory personnel. The load bank for the multiple output loads operating at + 2000 VDC cannot be adjusted when the loads are floating above ground since voltage insulation has not been added to the switch elements.

The beam and arc supply load banks can only simulate zero to full load and a short circuit. Provisions have not been made to go into a gradual overload because of expense for the high current components for the arc load and the high current, and voltage components for the beam supply. Figure 5 - 40 Laboratory facility shows the load banks around the breadboard and not integrated into a complete test unit in order to reduce the cost of test equipment and maximize the effort on the power processor development.

10.0 ENGINE INTEGRATION

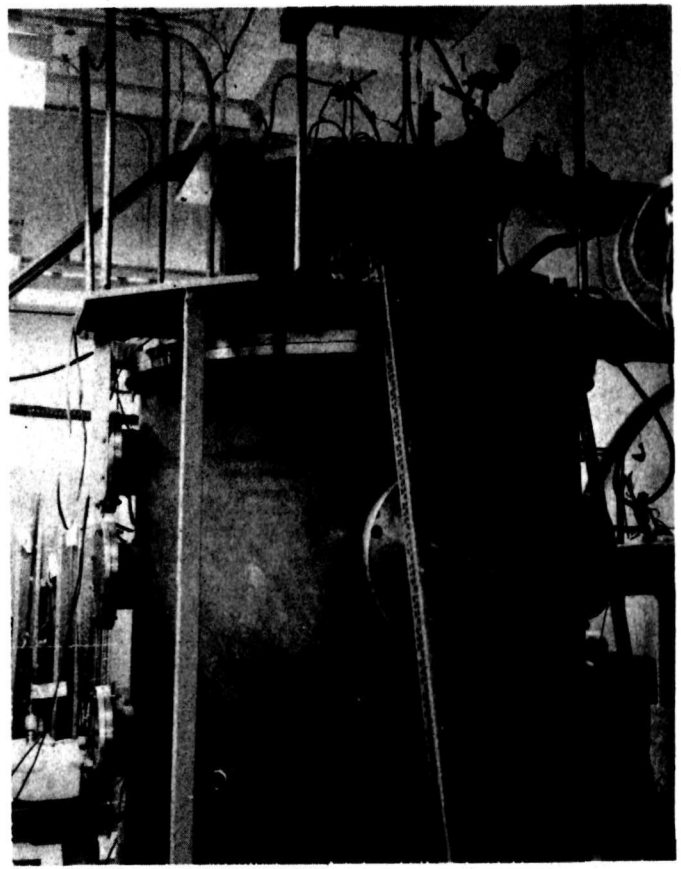
The hollow cathode ion engine without the neutralizer system was received from JPL and mounted in the vacuum chamber at TRW Systems. Figure 10-1 shows the ion engine test facilities including all the voltage and current instrumentation and laboratory power supplies. Particles had flaked off the interior of the laboratory engine, lodged between the beam and accelerator electrodes and presented a short circuit to the laboratory supplies. The engine was removed from the tank and cleaned. The engine was returned to the vacuum tank and the startup proceedure for the ion engine was determined, using laboratory supplies. During the beam startup, the engine presents a short between V5 and V6 electrodes which can be eliminated in either of two methods.

- Reduction of the magnets supply V1, or
- Reduction of the arc supply current limit.

The power processor beam and accelerator supply was substituted for the laboratory supplies and system operated for approximately 20 hours.

The beam supply operated over the input voltage range of 200 to 400 VDC and with beam currents of 0.25 amp to 1.0 amp and under overload condition without any problems.

TEST CONSOLE



VACUUM CHAMBER

FIGURE 10-1 ION ENGINE TEST FACILITY

The arc supply was also integrated with the engine to check for interaction and observe performance of the ion engine with the arc, beam and accelerator supplies which account for about 93% of the total electrical input power to the ion engine.

The ion engine experienced shorts which caused the beam and accelerator supply to go into current limiting mode of operation until the V_1 or V_4 supplies were adjusted at which time the high voltage returned to normal. Efficiency measurements using the test facility instrumentation were 91% for the arc, beam, and accelerator supplies which include all control power for the supplies.

The combination of the arc, beam and accelerator supplies of the power processor operated approximately 10 hours. During all these tests, there were no failures of the power processor, but there were some failures of the test facility instrumentation due to high peak currents during overloads and due to voltage transients.

As a result of these tests, it is expected that complexity of the command and protection system could be reduced.

11.0 NEW TECHNOLOGY

During this reporting period, new technology was developed in the following areas.

- o SCR inverter power stage
- o Multiple output regulator system

The addition of the center tap series inductor to the power stage provided a positive back bias condition for the auxiliary SCR and eliminated the forward dv/dt condition.

In the multiple output regulators, the ASDTIC controller when operating in a constant frequency system became unstable at certain duty cycles. To eliminate this instability an additional ramp function was summed with the integrator output signal to change the power stage gain as discussed in Section 5.5.11.

12.0 CONCLUSIONS

This program has demonstrated the feasibility of an electric propulsion power processor design using high voltage and high power silicon-controlled rectifiers (SCR's) as the main power switching elements operating over the wide input voltage range of 200 to 400Vdc. The SCR series resonant inverter has also demonstrated the ability to control the load current and thereby protect the power processor components from damage when overloads occur in the ion engine due to internal arcing. Since the component stresses are continuously under control by the LC resonant tank during startup, steady-state and overload modes of operation, the series inverter provides inherent ruggedness for all conditions of engine operation including severe engine arcing or shorts.

The power SCR's can operate at higher switching frequencies without efficiency or reliability penalties. Since the components are passing sinewave currents, there are no switching losses during turn-on of the SCR's, and since the LC resonant tank provides self-commutation, the SCR's are reliably turned off.

Continued development work is recommended to reduce weight by operation at even higher switching frequencies, to reduce part count by the use of high noise immunity integrated circuits, and to integrate the complete power processor with all its controls with the ion engine in order to determine interface requirements between the power source, power processor, ion engine and spacecraft.

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